SERVICE MANUAL

Design and specifications are subject to change without prior notice. (Only for Reference)

Description: SERVICE MANUAL 3M35G	
Version:V00.00	
Prepared By:	**Date:**
Checked By:	**Date:**
Approved By:	**Date:**

CONTENT

Revision History

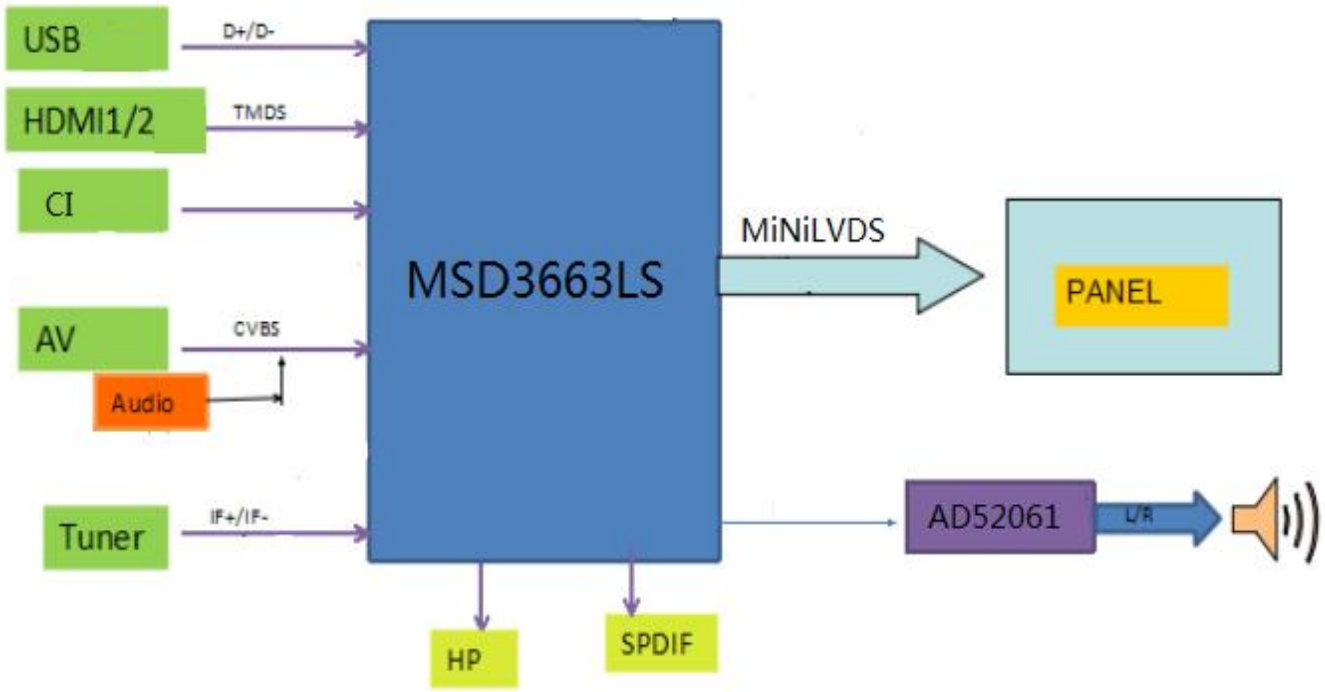
Version Number	Revision Data	Description of changes

1. Technical Specification

1	**Brief Information**					
1.1	Model Name					3M35G
1.2	Solution					MSD3663LS
1.3	Display Definition (max)					697.685*392.256
1.4	Display Interface	LVDS/MiniLVDS/EPI/EDP/V-BY-ONE				LVDS
1.5	AC Input Range	(三合一板必须填写)				100~240V
1.6	Standby Power Consumption					<0.5W
1.7	White Balance, Color Temperature	Min	TYP	Max	Unit	12500(266,276) 9800(280,290) 6500(313,329)
		6500	9800	12500	kdeg	
1.8	Video Noise Limited Sensitivity(@S/N=30dB)			60	dB	VHF
				60	dB	UHF
1.9	Video Input Level(75 ohm)		1		Vp-p	
2	**Signal Receiving System**					
2.1	**ATV Receiving System**	**ATV Receiving System**				
2.1.1		NTSC-M				No
2.1.2		PAL BG/I/DK/NTSC-M				No
2.1.3		PAL/SECAM BG/DK/I SECAM L/L"				PAL/SECAM BG/DK/I
2.1.4		PAL M/N NTSC-M				No
2.2	**DTV Receiving System**	**DTV Receiving System**				
2.2.1		ATSC				No
2.2.2		DVB-T				No
2.2.3		DVB-T with CI				YES
2.2.4		DVB-T2				No
2.2.5		DVB-T2 with CI+				YES
2.2.6		ISDB-T/SBTVD-T				No
2.2.7		DTMB				No
2.2.8		DVB-C with CA				No
2.2.9		DVB-S				YES
2.2.10		DVB-S2				YES
2.3	**Antenna input**	**Antenna input**				
2.3.1		Antenna Input port: 1 (1 for analogue)				No

2.3.2		Antenna Input port: 1 (1 for both analogue and digital)	YES
2.3.3		Antenna Input port: 2 (1 air + 1 Cable)	No
2.3.4		Type of Antenna Input Port	IEC Female
2.3.5		Receiving Frequency range (ATV)	47.25MHz～865.25MHz
2.3.6		Receiving Frequency range (DTV)	177.5-858MHZ
2.37		Receiving Frequency range (DVB-S/S2)	

2. System Block



3. List of key parts

（三合一板需要加入电源部分关键器件）

NAME	Part reference	DESCRIPTION	SKYWORTH P/N
IR Recevier	IR1	SMD MODULE 38KHZ	5300-14841A-0S00
Crystal	X0T9	SMD CRYSTAL 27.000000MHZ HC-49/USM	492L-127054-QS00
	X0T8	SMD CRYSTAL 24.000MHZ +/-20PPM 8PF HC-49	4900-124052-RZ00
	Y201	SMD CRYSTAL 24.000MHZ +/-20PPM 20PF HC-49	4900-124053-R000
Tuner	U1T4	Si2151 TV TUNER	471J-S21510-0240
	U0T1	AV2017	47EY-A20170-0200
IC	U201	MSD3663LS MSTAR (TV CONTROLLER)	475C-M36630-2160
	U0M1	GD25Q64CSIG	47F2-G25641-0080
	U0A4	AD52061	
	U0N1	TPS65162RGZR TI	4722-T65160-0480
	U0P8	MP1653GTF-Z	476A-M16530-0060
	U0P4 U0P9	MP1652GTF-Z	476A-M16520-0060
	U0T5	RT5047GSP	472L-R50471-0080
	U0D1	LNK6778K-TL PI	4785-L67780-0120
	U0B1	OZ560EGN-B1-0-TR	476K-Z56000-0160
OTHERS			

4. IC General Description

(选取部分对售后有帮助的 IC,截取关键内容，不要整份规格书粘贴，截图要清晰，放大后能看清楚所有文字，三合一板需要加入电源 IC 和背光 IC 的介绍)

4.1 Main IC: MSD3663LS

Attention Please: Under the technology license agreement between MStar and Dolby/DTS/Microsoft, MStar is obliged not to provide samples that incorporate Dolby/DTS/Microsoft technology to any third party who is not a qualified licensee of Dolby/DTS/Microsoft respectively.

FEATURES

MSD3663LSAT is a highly integrated single chip solution for digital DVB-C/DVB-T/DVB-T2/ISDB-T/DVB-S/ DVB-S2 TV system. Key features include:

1. *DVB-C/DVB-T/DVB-T2/ISDB-T/DVB-S/DVB-S2 and Analog TV Front-End Demodulator*
2. *Multi-Standard A/V Decoder*
3. *MStar High Performance Video Processor*
4. *Home Theater Sound Processor*
5. *Embedded Memory for optimized BOM cost*
6. *Multiple HDMI 1.4 Compliant Ports with ARC Support*
7. *One MHL 2.1 Compliant Port*
8. *Transport-Stream Input for Extended DTV System*

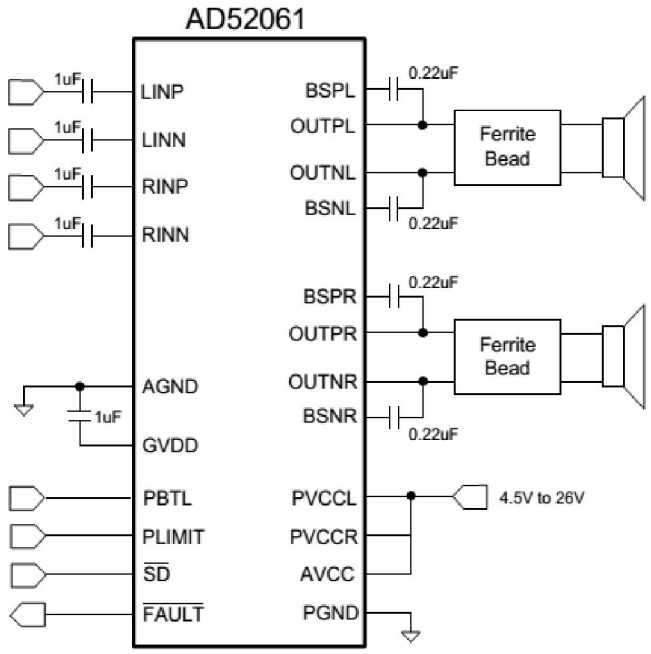
- High Performance Micro-processor
  - MIPS34Kf with 32KB/32KB I/D cache
  - Supports Hardware floating point unit
- HEVC/H.265 Video Decoder
  - Supports HEVC/H.265 video decoding
  - Supports Main/Main-10 profile, level 4.1, high tier
  - Supports 8-bit/10-bit color depth
  - Supports resolution up to 1920x1080@60fps
  - Supports max bitrate upto 50 Mbps
- AVC/H.264 Video Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding
  - Supports resolution up to 1920x1080@60fps
  - Supports bitrate up to 62.5Mbps, the upper limit of level 4.2
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@30fps
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p, 1080i, 720p) and SDTV
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@30fps)
  - Supports DivX Home Theater & HD profiles
  - Supports FLV version1 video format decoding
- AVS/AVS+ Video Decoder Optional
  - Supports Broadcasting profile, level 6.0.1.08.60 (AVS+)
  - Supports Jizhun profile, level 6.0
  - Supports bitrate up to 50Mbps
  - Supports resolution up to 1920x1080@30fps
- RealMedia Video Decoder Optional
  - Supports RV8, RV9, RV10 decoders
  - Supports file formats with RM and RMVB
  - Supports maximum resolution up to 1080p@30fps
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame
- Hardware JPEG Decoder
  - Supports upto 640x480@30fps
  - Supports formats: 422/411/420/444/422T
  - Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
  - Supports both color and grayscale pictures
  - Supports sequential mode, single scan
  - Supports programmable Region of Interest (ROI)
  - Following the file header scan the hardware decoder fully handles the decode process

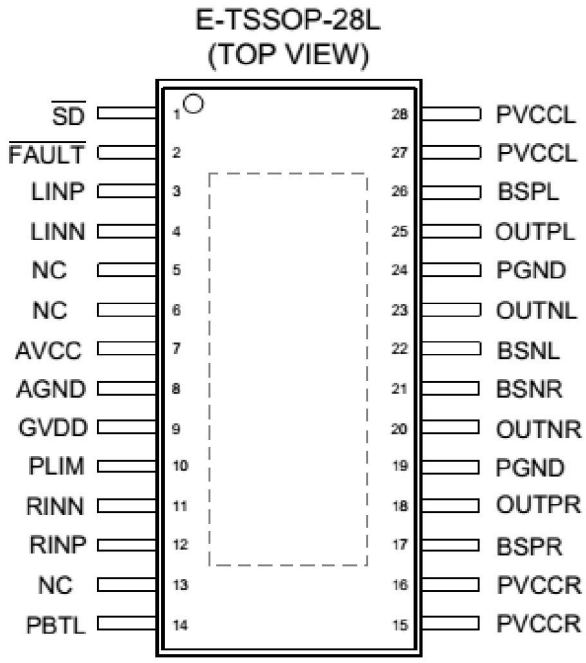
- VC-1 Video Decoder[Optional]
  - Supports SMPTE-421M (WMV video) decoding up to MH@HL
  - Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p30)
- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
  - Automatic standard detection
  - Motion adaptive 3D comb filter
  - One configurable CVBS & Y/C S-video input
  - Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), and V-chip and SCTE
- Multi-Standard TV Sound Processor
  - Supports BTSC/A2 demodulation
  - Supports NICAM/FM/AM demodulation
  - Supports MTS Mode Mono/Stereo/SAP in BTSC mode
  - Supports Mono/Stereo/Dual in A2/NICAM mode
  - Built-in audio sampling rate conversion (SRC)
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
  - Advanced sound processing options available, for example: Dolby[1], DTS[2]
  - Supports digital audio format decoding:
    - MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3) [Optional], AAC-LC, HE-AAC, WMA and supports Dolby Digital Plus [Optional]
  - Supports Audio Description
  - Supports programmable delay for audio/video synchronization
- Audio Interface
  - Two L/R audio line-inputs and two mono Mic. Inputs
  - One L/R outputs for main speakers, monitor output, and SCART output
  - Supports stereo headphone driver
  - I2S digital audio output
  - S/PDIF digital audio output
  - Supports HDMI receiver ARC function
- Analog RGB Compliant Input Ports
  - Three analog ports support up to 1080P
  - Supports PC RGB input up to SXGA@75Hz
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG Sync-on-Green
  - Automatic color calibration
- Analogue RGB Auto-Configuration & Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync Detection for H/V Sync
- DVI/HDCP/HDMI Compliant Input Ports
  - Three HDMI/DVI Input ports
  - HDMI 1.4a Compliant
  - HDCP 1.4 Compliant
  - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
  - Supports CEC
  - Supports HDMI 3D format input
  - Supports UHD 30Hz down-scaling
  - Supports HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
  - Embedded HDCP key
- HDMI/MHL Dual-Purpose Port
  - MHL 2.1 Compliant
  - MHL/HDMI Auto-detection
  - Supports MHL charging in normal/standby mode

Power Pins

Pin Name	Pin Type	Function	Pin
AVDD_5V	5V Power	Analog 5V Power	206
AVDD33_DADC	3.3V Power	Demod ADC Power	52
AVDD33_DMPLL	3.3V Power	Crystal Power	59
AVDD33_AU	3.3V Power	Audio Power	38
AVDD33_ADC	3.3V Power	Video ADC Power	24
AVDD33_EAR	3.3V Power	Earphone Driver Power	49
AVDD33_ETH	3.3V Power	Ethernet Power	192
AVDD_MOD	3.3V Power	MOD 3.3V Power	9, 73, 153, 186
VDDIO_CMD	1.5V Power	DDR Command Power	69
VDDIO_DATA	1.5V Power	DDR Data Power	187, 189
VDDIO_DRAM	1.5V Power	DDR DRAM Power	191, 190
DVDD_DDR_DATA	V_{VDD_core}	DDR DATA Power	185
VDDC	V_{VDD_core}	Digital Core Power	37, 62, 70, 162, 169, 177, 208
AVDDL_MOD	V_{VDD_core}	MOD Power	162
AVDDL_DVI	V_{VDD_core}	DVI Power	208
GND	Ground	Ground	188, 197

4.2 Amplifier: AD52061





Pin Description

NAME	E-TSSOP -28L	TYP	DESCRIPTION
$\overline{SD}$	1	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	2	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{FAULT}$ pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	3	I	Positive audio input for left channel. Biased at 2.5V.
LINN	4	I	Negative audio input for left channel. Biased at 2.5V.
NC	5	NA	NC pin
NC	6	NA	NC pin
AVCC	7	P	Analog supply.
AGND	8	P	Analog signal ground. Connect to the thermal pad.
GVDD	9	O	5V regulated output, also used as supply for PLIMIT function.
PLIMIT	10	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	11	I	Negative audio input for right channel. Biased at 2.5V.
RINP	12	I	Positive audio input for right channel. Biased at 2.5V.
NC	13	NA	NC pin
PBTL	14	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
PVCCR	15,16	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	17	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
PGND	19	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
PGND	24	P	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	27,28	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
Thermal Pad		P	Must be soldered to PCB's ground plane.

4.3 RF controller: Si2151-A10-GRM

Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVB-T2/T/C2/C, ISDB-T/C, DTMB
  - 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
  - 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™ DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High WiFi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V single-supply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

Ordering Information:
See page 26.

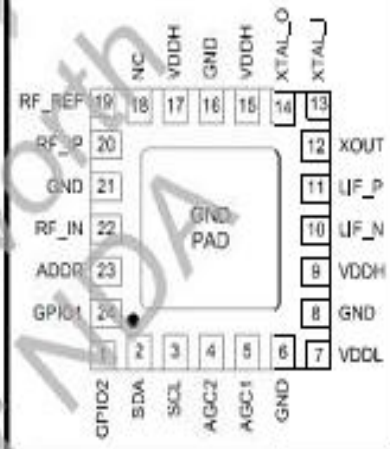
Applications

- Hybrid 1/2-NIM tuner module
- iDTV (Integrated Digital TV)
- Hybrid terrestrial and cable STB
- Hybrid PVR and BDR recorder
- PC-TV accessories

Description

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Pin Assignments



Patents pending

Functional Block Diagram

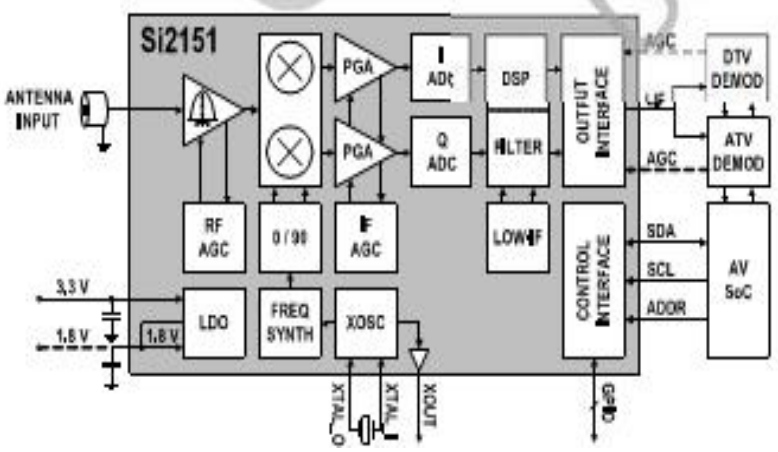
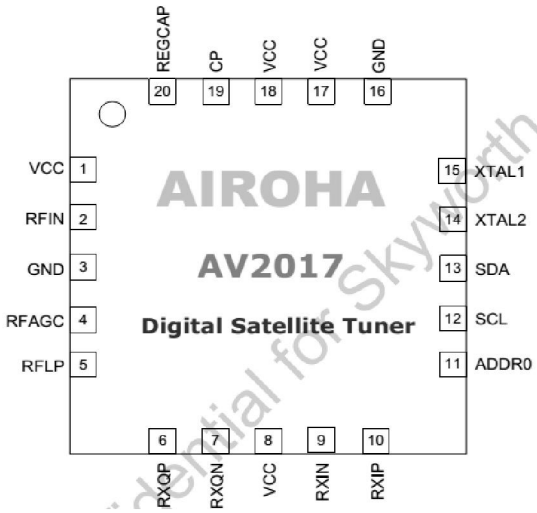


Table 13. Si2151 Pin Descriptions

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I²C data input/output
3	SCL	I	I²C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I²C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

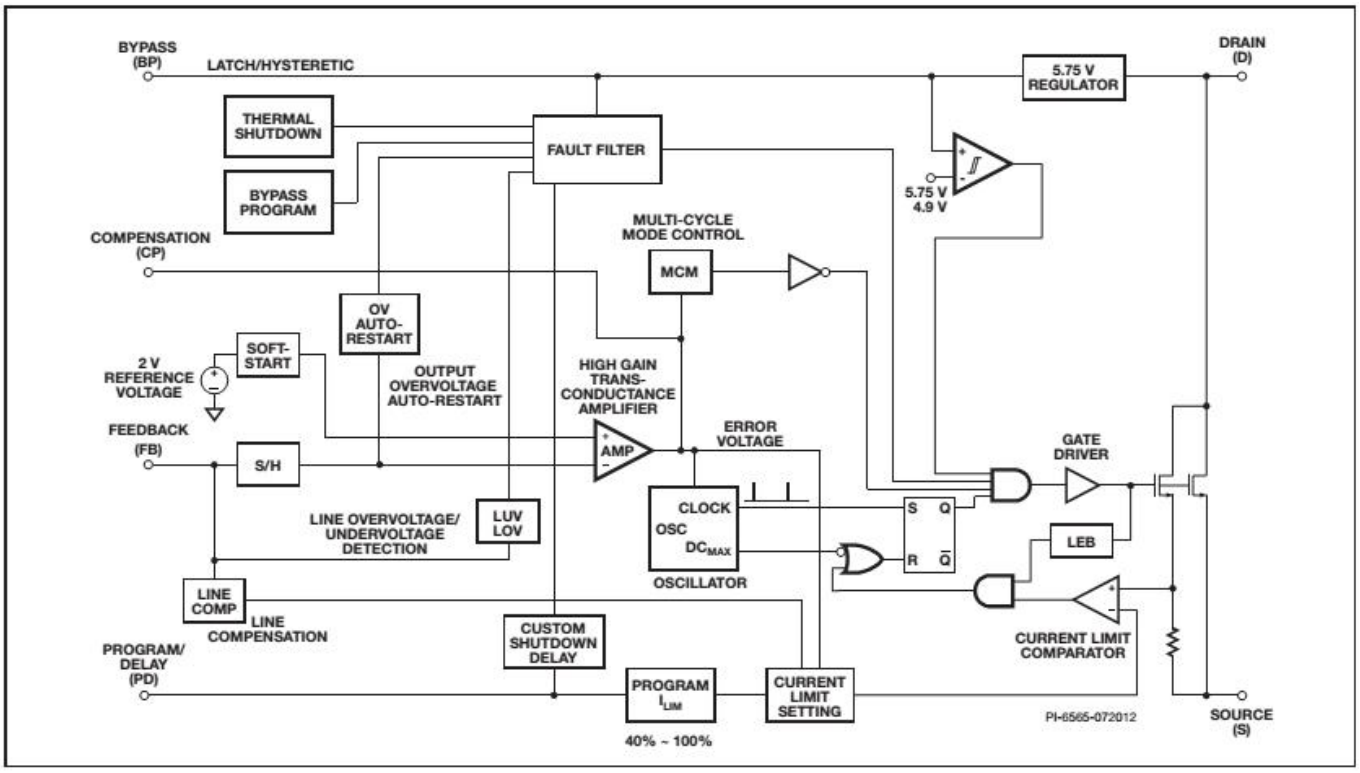
4.4 RF controller: AV2017 (DVB-S/S2)



Pin Name Description

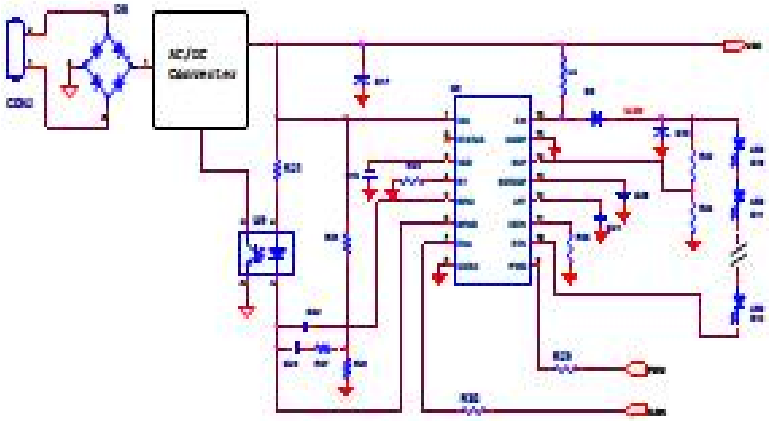
PIN	SIGANL	TYPE	DESCRIPTION
1	VCC	VCC Supply	3.3V Supply Voltage for Regulator
2	RFIN	Input, Analog	RF Signal Input
3	GND	Ground	Ground
4	RFAGC	Input, Analog Control	RF AGC Control Voltage
5	RFLP	Output, Analog	RF Loop Through Signal Output
6	RXQP	Output, Analog	BB Output
7	RXQN	Output, Analog	BB Output
8	VCC	VCC Supply	3.3V Supply Voltage for Regulator
9	RXIN	Output, Analog	BB Output
10	RXIP	Output, Analog	BB Output
11	ADDR0	Digital	Device Address Control
12	SCL	Input, Digital	Serial Interface
13	SDA	Input/Output, Digital	Serial Interface
14	XTAL2	Analog	XTAL Output
15	XTAL1	Analog	XTAL Input
16	GND	Ground	Ground
17	VCC	VCC Supply	3.3V Supply Voltage for Regulator
18	VCC	VCC Supply	3.3V Supply Voltage for Regulator
19	CP	Analog	Charge Pump
20	REGCAP	Analog	Regulator Output for External Capacitor

4.5 POWER IC LinkSwitch-HP

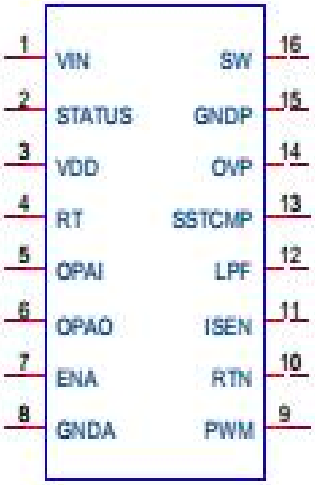


4.6 High Power LED Driver Controller

SIMPLIFIED APPLICATION DIAGRAM



PIN DIAGRAM



PIN DESCRIPTION:

Pin NO.	Name	I/O[1]	Description
1	VIN	---	Power supply of IC
2	STATUS	O	Fault Status ouput
3	VDD	I/O	Internal 6V voltage regulator output
4	RT	I/O	Resistor to set the IC Operation Frequency
5	OPAI	I	Input of Built-In Shunt Regulator
6	OPAO	I/O	Output of Built-In Shunt Regulator
7	ENA	I	ON/OFF Control of the LED driver
8	GNDA	-	Signal GND of IC
9	PWM	I	External PWM Dimming Signal Input
10	RTN	I/O	Drain of internal LED current switch
11	ISEN	I/O	Source output of LED current switch and LED current sense pin
12	LFP	I/O	Low pass filter for analog dimming and selection between analog dimming and direct PWM dimming modes
13	SSTCMP	I/O	Soft start and compensation for LED driver control loop
14	OVP	I	Over voltage protection sense input
15	GNDP	---	Power GND of IC
16	SW	O	Drain of power MOSFET for boost converter

Note[1]: I=Input, O=Output, I/O=Input/Output

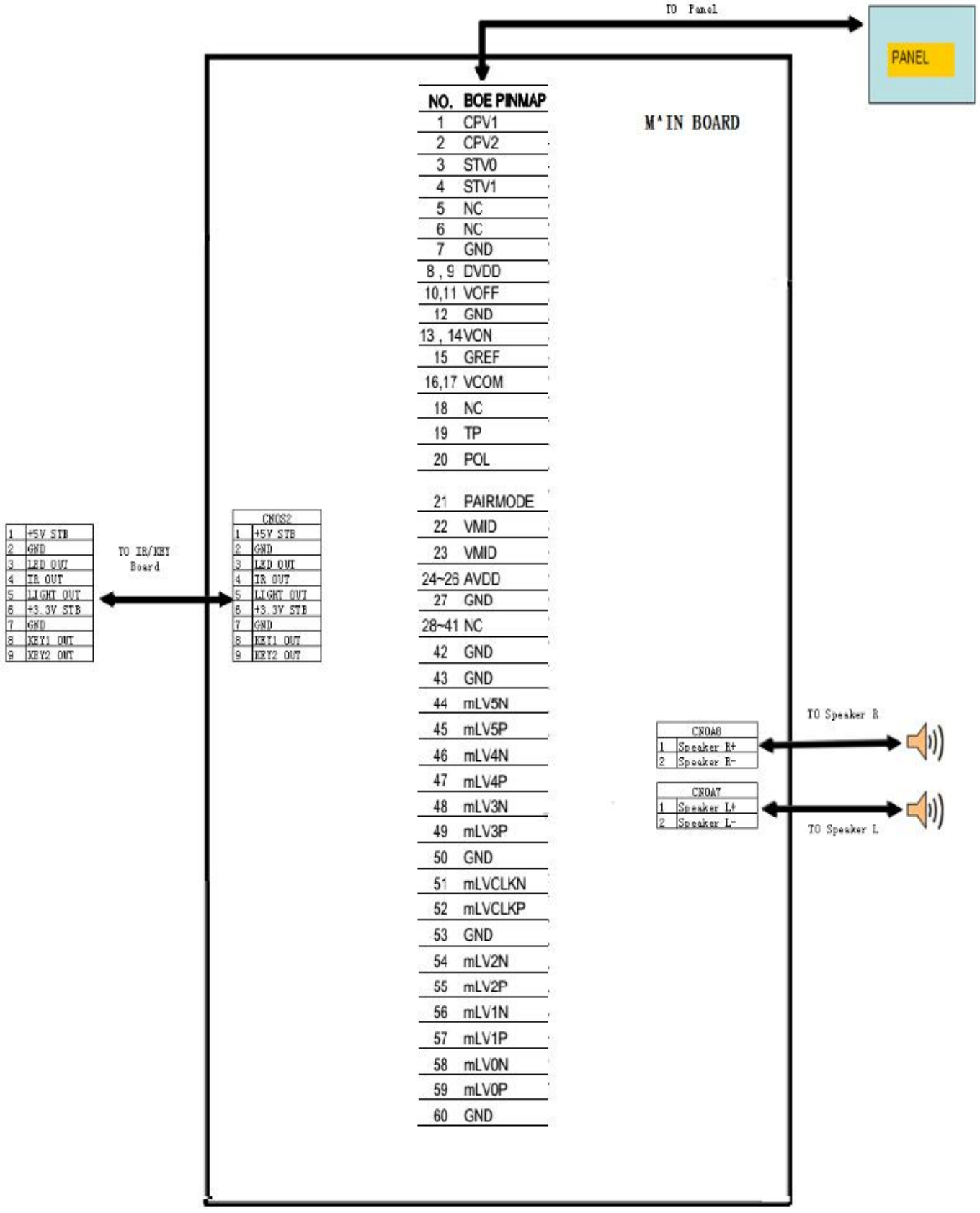
5.Software Upgrade

>USB upgrade guide

1. Uncompress the file to the root of the U disc
2. Plug U disck into USB(2.0)
3. Open the TV, press Menu key, choose Option-SW Upgrade(USB), then choose yes,
4. Do don't switch off the TV before the update is fininished.

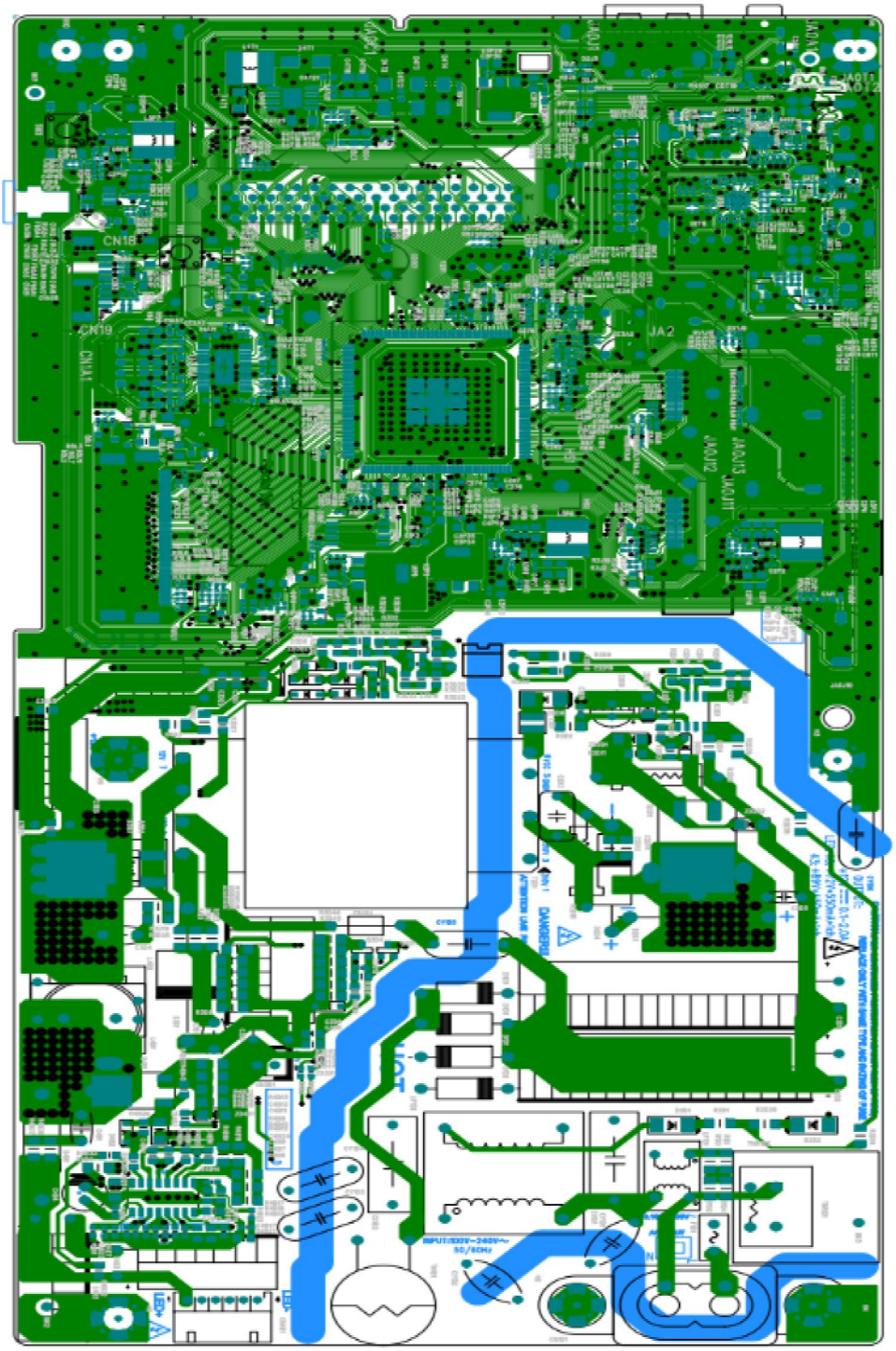
6.Setting Hotle Mode Menu

7.Wiring Diagram

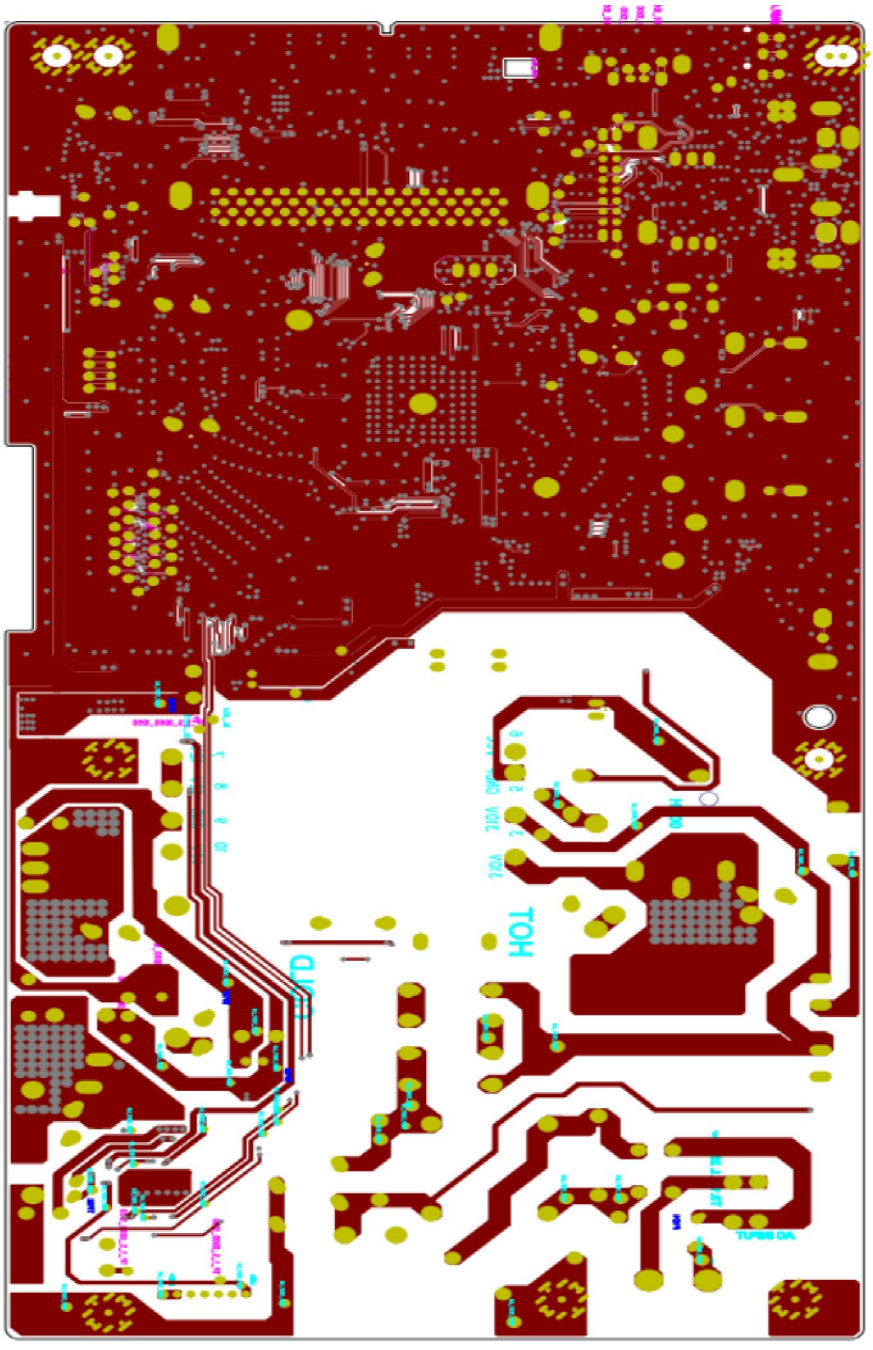


8. PCB Silkscreen

8.1 Silkscreen top



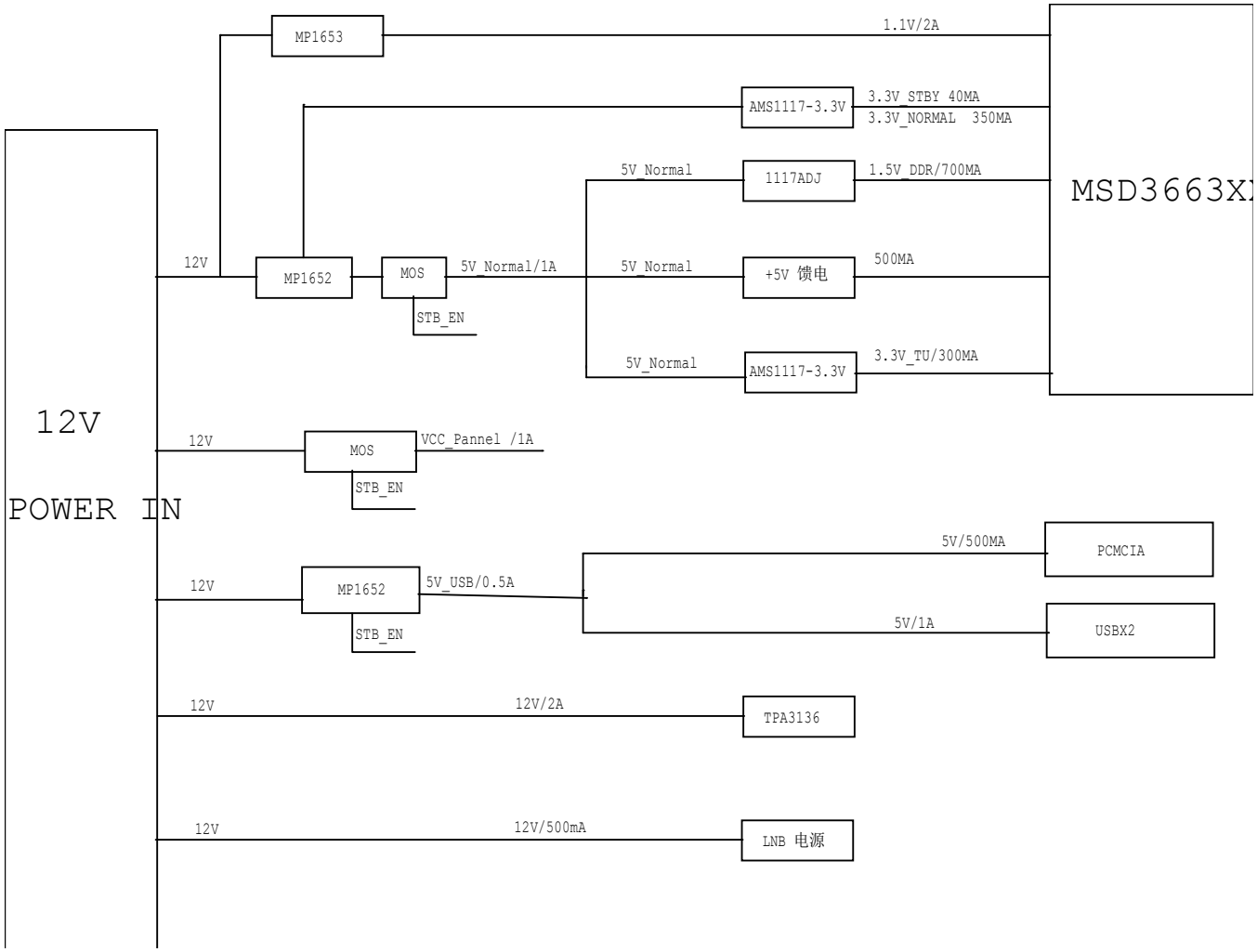
8.2 Silkscreen bottom



9.Schematic Circuit Diagram

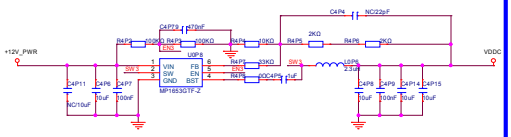
Page00 Power Tree

Page1 Power Circuit


12V
POWER IN
MP1653
1.1V/2A
AMS1117-3.3V
3.3V_STBY 40MA
3.3V_NORMAL 350MA
5V_Normal
1117ADJ
1.5V_DDR/700MA
MSD3663X
12V
MP1652
MOS
5V_Normal/1A
STB_EN
5V_Normal
+5V 馈电
500MA
5V_Normal
AMS1117-3.3V
3.3V_TU/300MA
12V
MOS
VCC_Pannel /1A
STB_EN
5V/500MA
PCMCIA
12V
MP1652
5V_USB/0.5A
STB_EN
5V/1A
USBX2
12V
12V/2A
TPA3136
12V
12V/500mA
LNB 电源

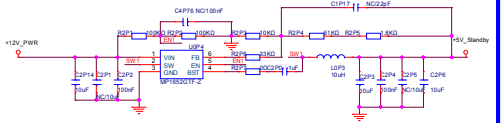
1.15V 2A for VDDC

1、+12V_NOR转+1.15V_VDDC

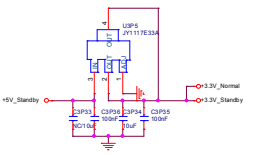


2、+12V_NOR转+5V_Standby

（DC-DC价格0.075USD 规格标称最大2A 500KHZ 输入电压范围4.7V-16V 轻载高效 优选）

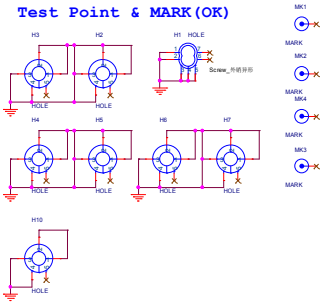


2、+5V_Standby转+3.3V_Standby



说明:1、这是一款固定输出电压的LDO.
2、PCB排版时输入电容和输出电容尽量靠近IC

Test Point & MARK(OK)

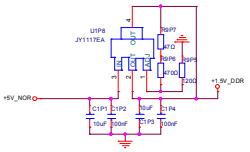


STANDBY >>STANDBY

8、LDO +5V_NOR转+1.5V_DDR

(优选 LDO价格0.1864RMB SOT-223 规格标称最大1A)

实际带载能力需要根据压降及Pcilt算，要考虑LDO的温升问题



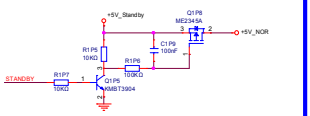
说明:1、这是一款可调节输出电压的LDO.
2、PCB排版时输入电容和输出电容尽量靠近IC　3、如果需要调节输出电压，可以根据公式计算。

Vout=1.25x(1+(R2/R1))

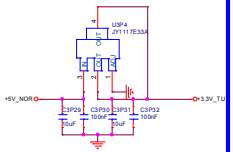
R1=R9P6+R9P7　　R2=R9P5

R1	R2	Vout
4100-CA1210-2205(120Ω+4100-CA0000-2205(0Ω)	4100-CA2210-2205(120Ω)	3.33V
4100-CA2010-2205(200Ω+4100-CA0000-2205(0Ω)	4100-CA2210-2205(120Ω)	2.5V
4100-CA2010-2205(200Ω+4100-CA6800-2716(6Ω)	4100-CA2210-2205(120Ω)	1.8V
4100-CA4710-2205(470Ω+4100-CA4100-2205(47Ω)	4100-CA2210-2205(120Ω)	1.5V

5V SWITCH

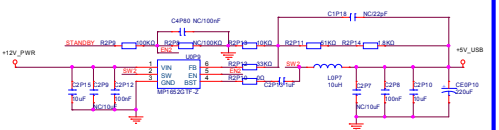


TUNER POWER



说明:1、这是一款固定输出电压的LDO.
2、PCB排版时输入电容和输出电容尽量靠近IC

3、+12V_NOR转+5V_NOR



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Size: Custom	Document Number: 01_Power Circuit		Rev: 1.0
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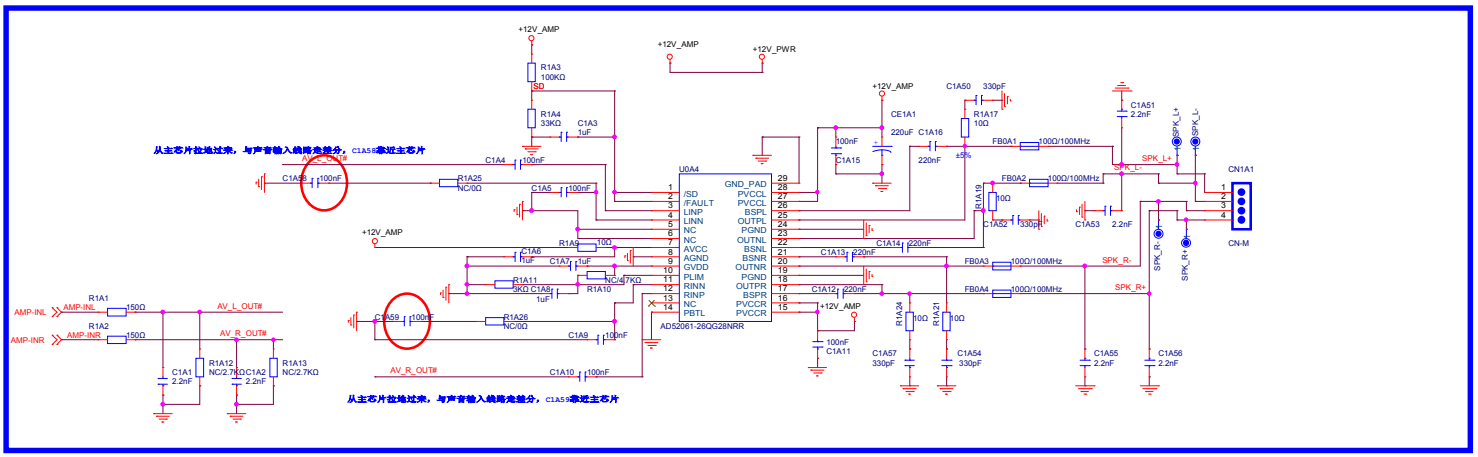
AUDIO AMP

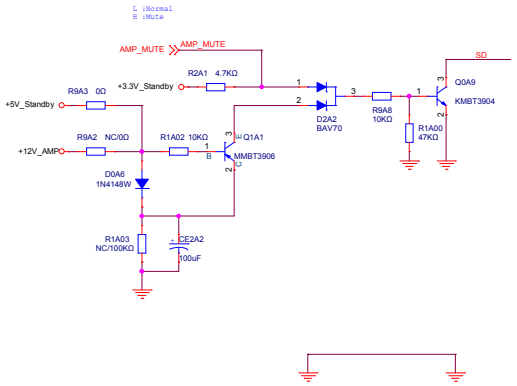


MUTE CONTROL

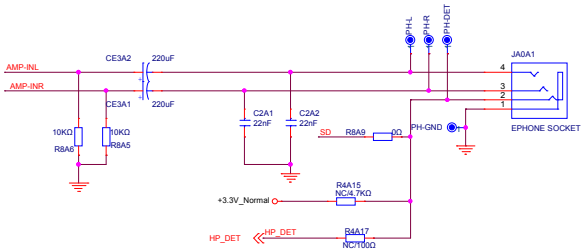
AMP_RST=0 MUTE

AMP_MUTE=0 MUTE

静音电路



EARPHONE OUT



SKYWORTH		
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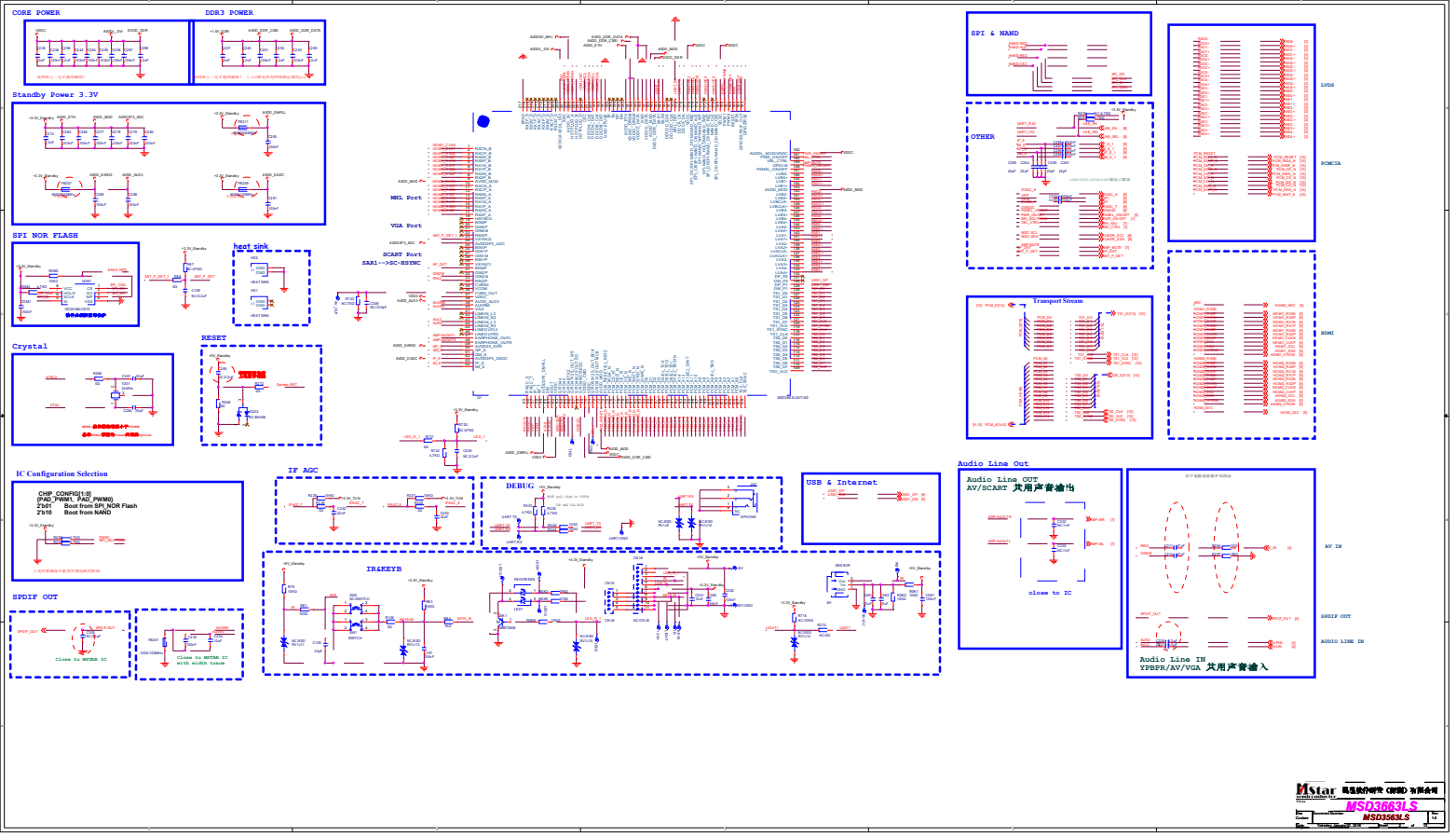
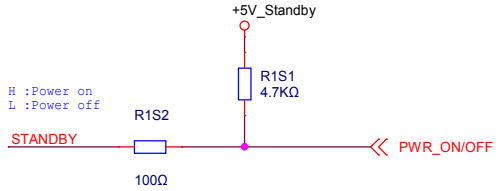
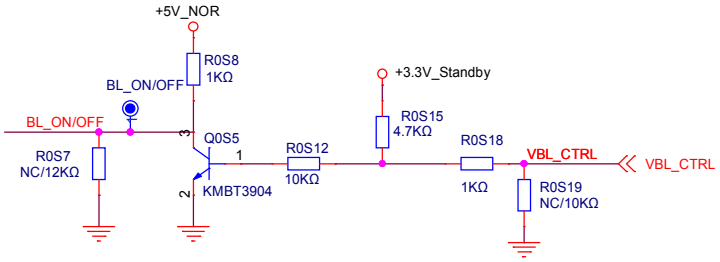

CORE POWER
DDR3 POWER
Standby Power 3.3V
SPI NOR FLASH
heat sink
Crystal
RESET
IC Configuration Selection
CHIP_CONFIG[1:0]
(PAD_PWM1, PAD_PWM0)
2'b01 Boot from SPI_NOR Flash
2'b10 Boot from NAND
SPDIF OUT
IF AGC
DEBUG
USB & Internet
IR&KEYB
SPI & NAND
OTHER
LVDS
PCMCIA
HDMI
Transport Stream
Audio Line Out
AV/SCART 共用声音输出
close to IC
AV IN
SPDIF OUT
AUDIO LINE IN
Audio Line IN
YPBPR/AV/VGA 共用声音输入
MSD3663LS
MSD3563LS

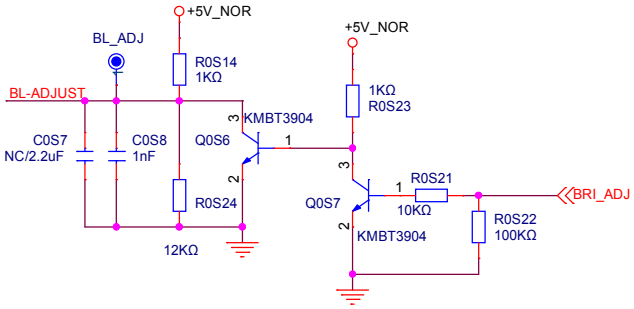
STANDBY → STANDBY

BL_ON/OFF → BL_ON/OFF

BL-ADJUST → BL-ADJUST







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Size: Custom	Document Number: <Doc>	Rev: <RevCode>
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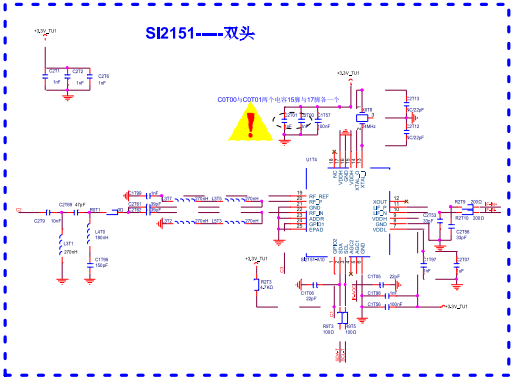
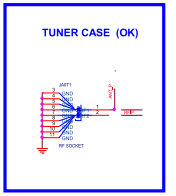
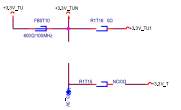
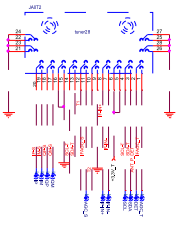
T SI TUNER (OK)



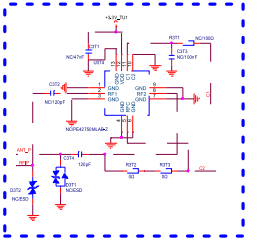
TUNER CASE (OK)



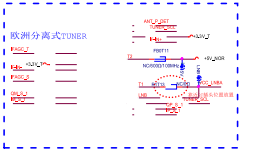




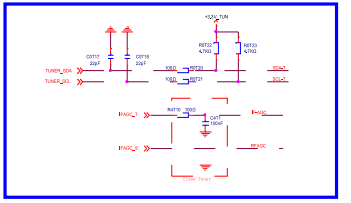
兼容ISDB



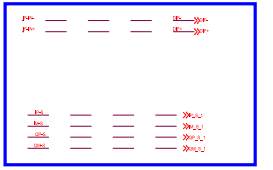
欧洲分离式TUNER



AGC RC Filter &I2C



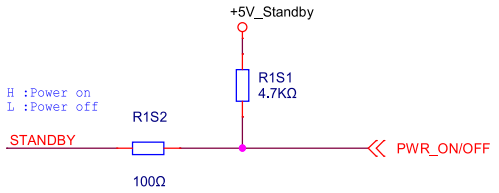
DVB-C/T/T2 /S/S2DIF

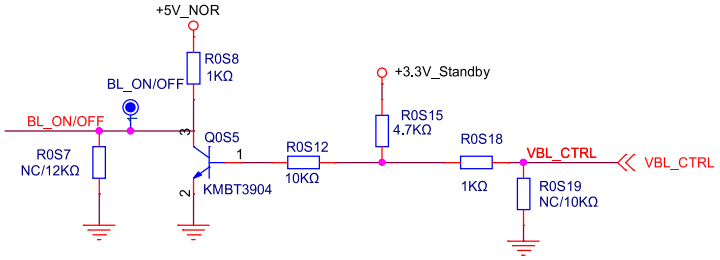


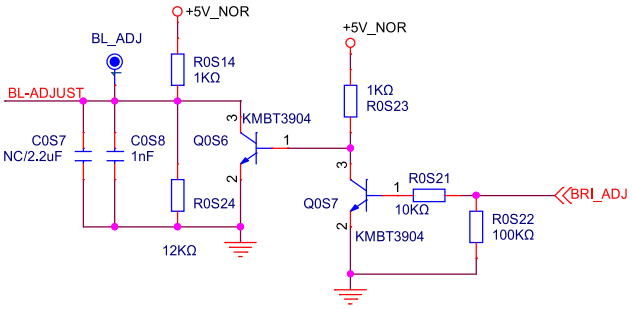
SKYWORTH

TUNER

STANDBY
BL_ON/OFF
BL-ADJUST







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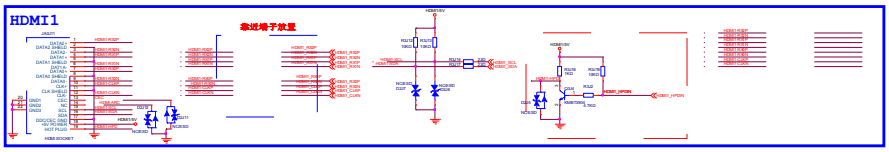
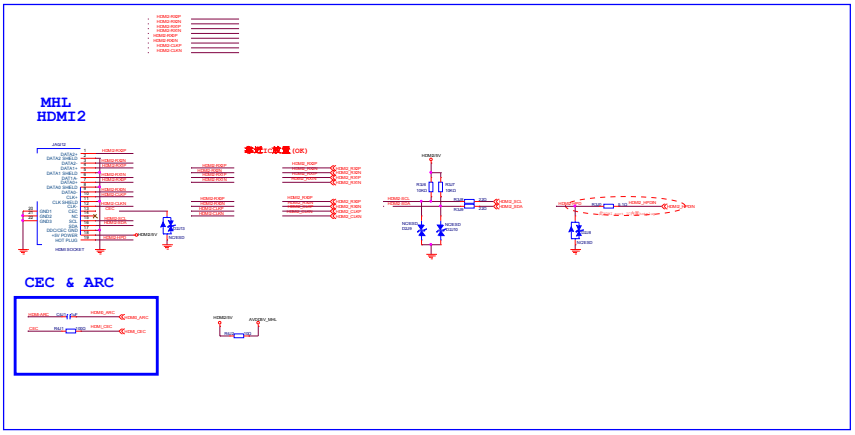
HDMI1

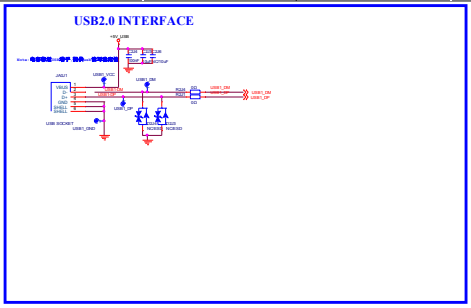


MHL HDMI2

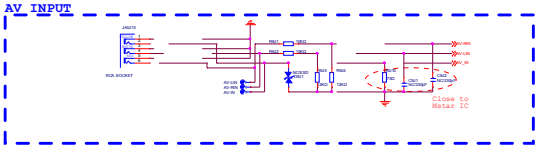


CEC & ARC

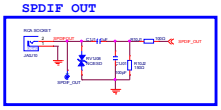
USB2.0 INTERFACE



AV INPUT

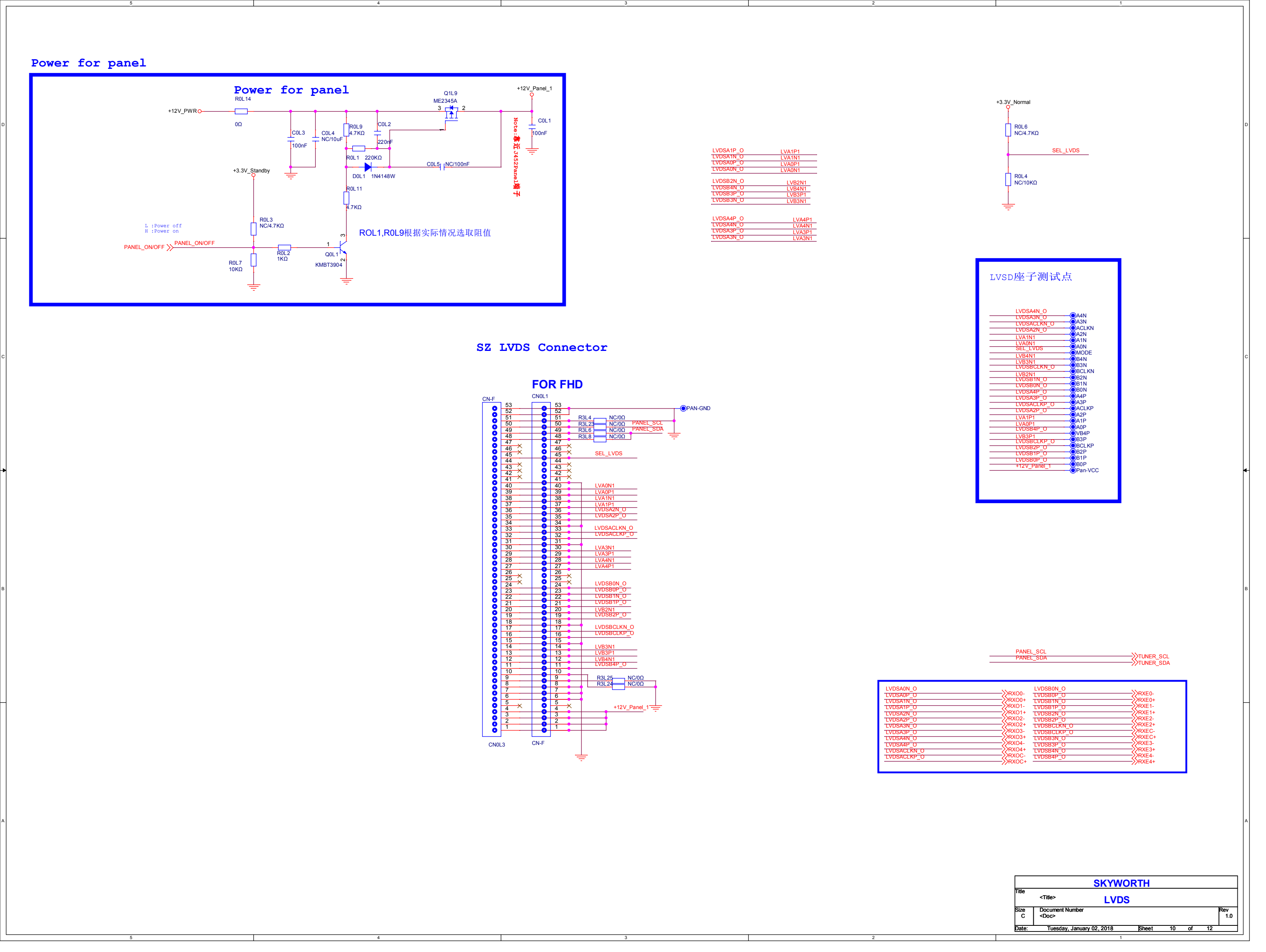


SPDIF OUT



SKYWORTH

STANDARD PORT


Power for panel
Power for panel
+12V_PWR
R0L14
0Ω
C0L3
100nF
C0L4
NC/10uF
R0L9
4.7KΩ
C0L2
220nF
Q1L9
ME2345A
+12V_Panel_1
C0L1
100nF
R0L1
220KΩ
D0L1
1N4148W
C0L5
NC/100nF
R0L11
4.7KΩ
+3.3V_Standby
R0L3
NC/4.7KΩ
L :Power off
H :Power on
PANEL_ON/OFF
R0L2
1KΩ
Q0L1
KMBT3904
R0L7
10KΩ
ROL1,R0L9根据实际情况选取阻值
+3.3V_Normal
R0L6
NC/4.7KΩ
SEL_LVDS
R0L4
NC/10KΩ
SZ LVDS Connector
FOR FHD
CN-F
CN0L1
CN0L3
PAN-GND
PANEL_SCL
PANEL_SDA
+12V_Panel_1
LVSD座子测试点
TUNER_SCL
TUNER_SDA
SKYWORTH
LVDS
Size C
Document Number <Doc>
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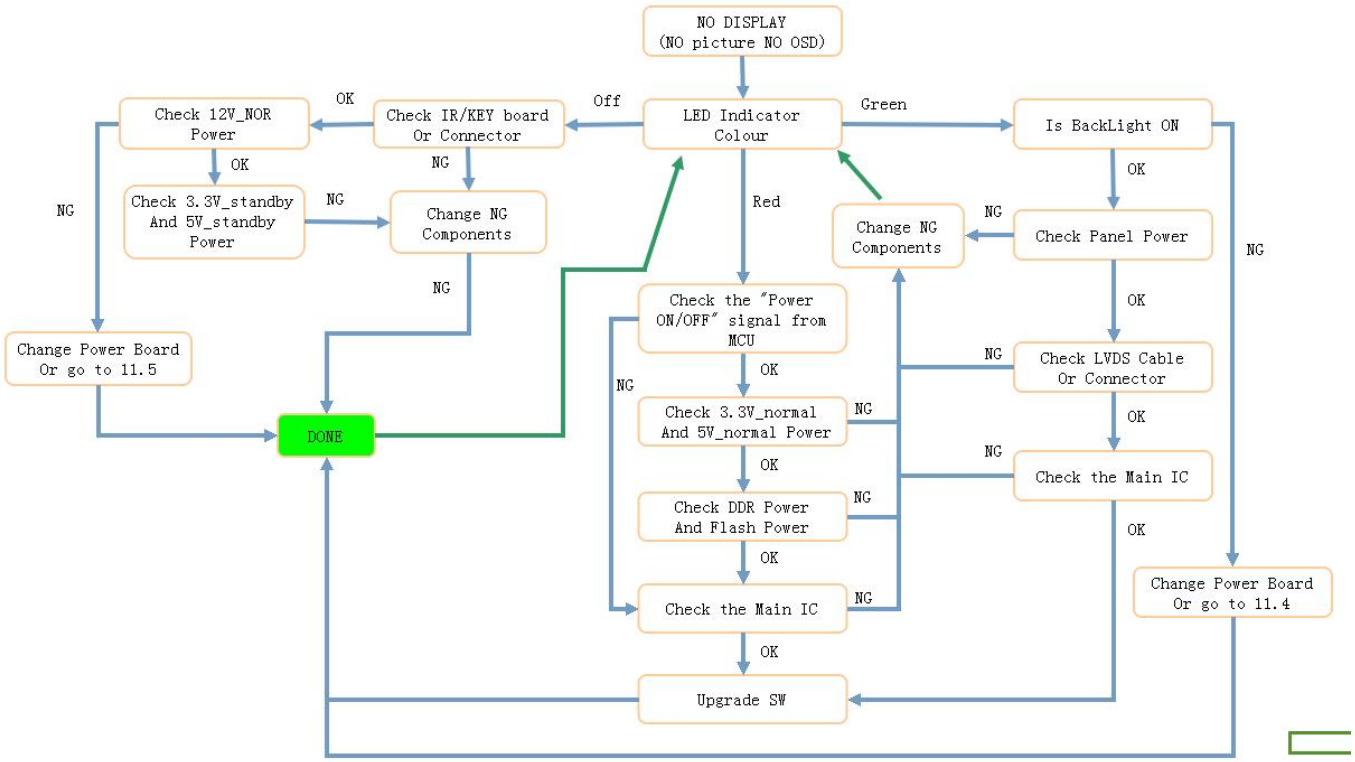
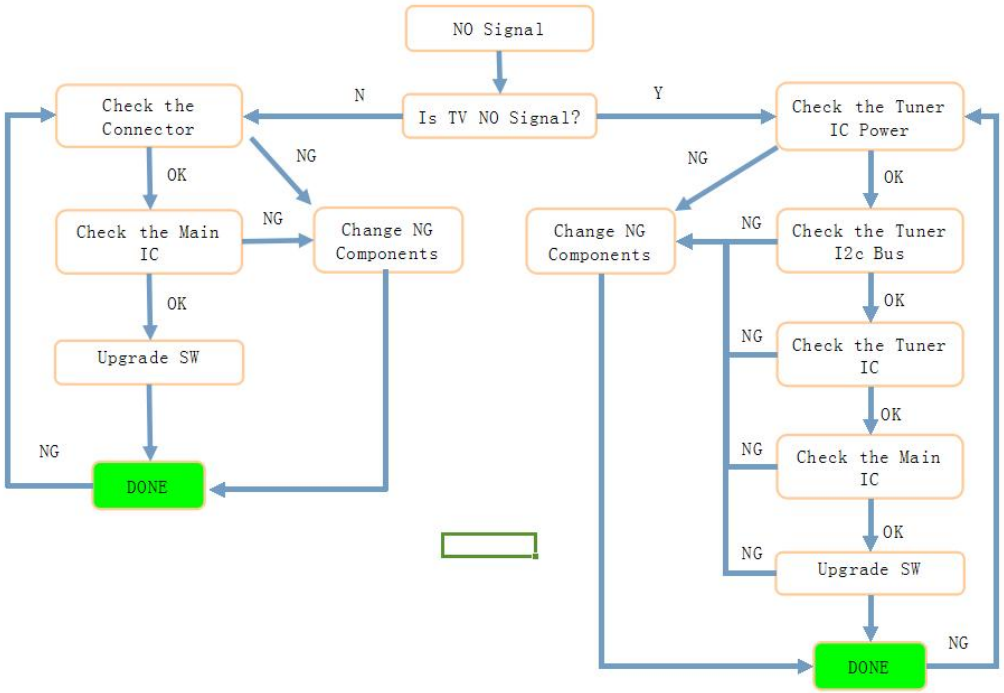
10.Trouble Shooting

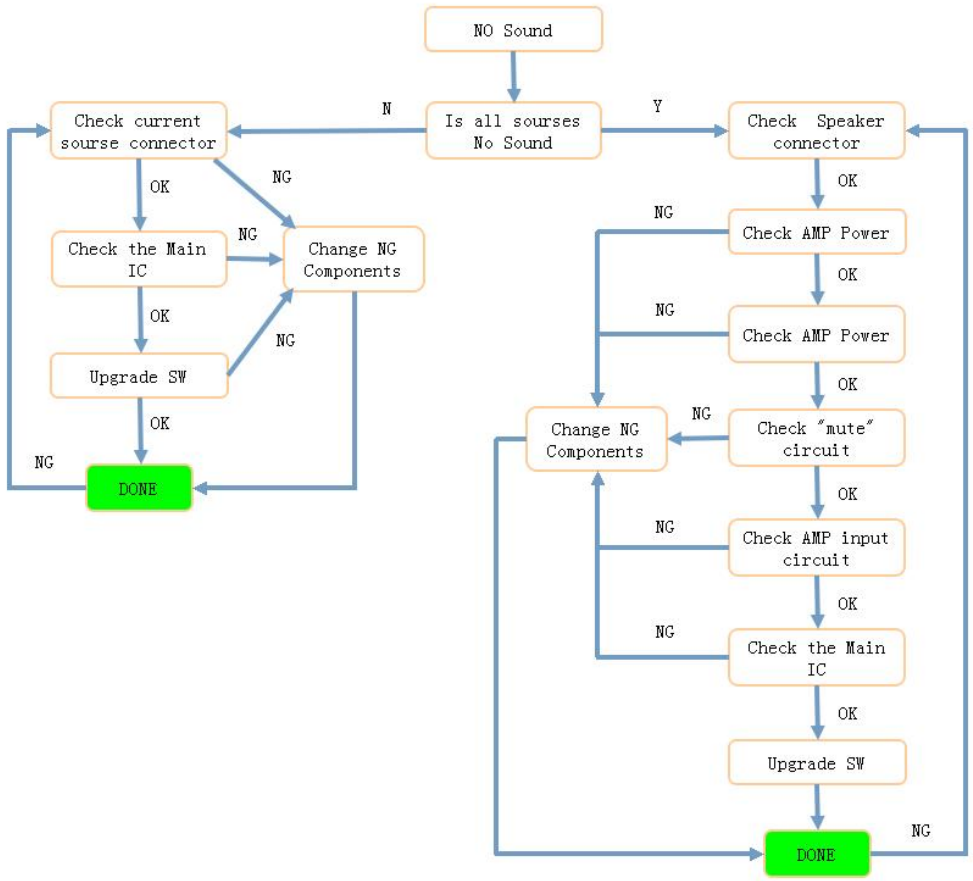
10.1 No Display



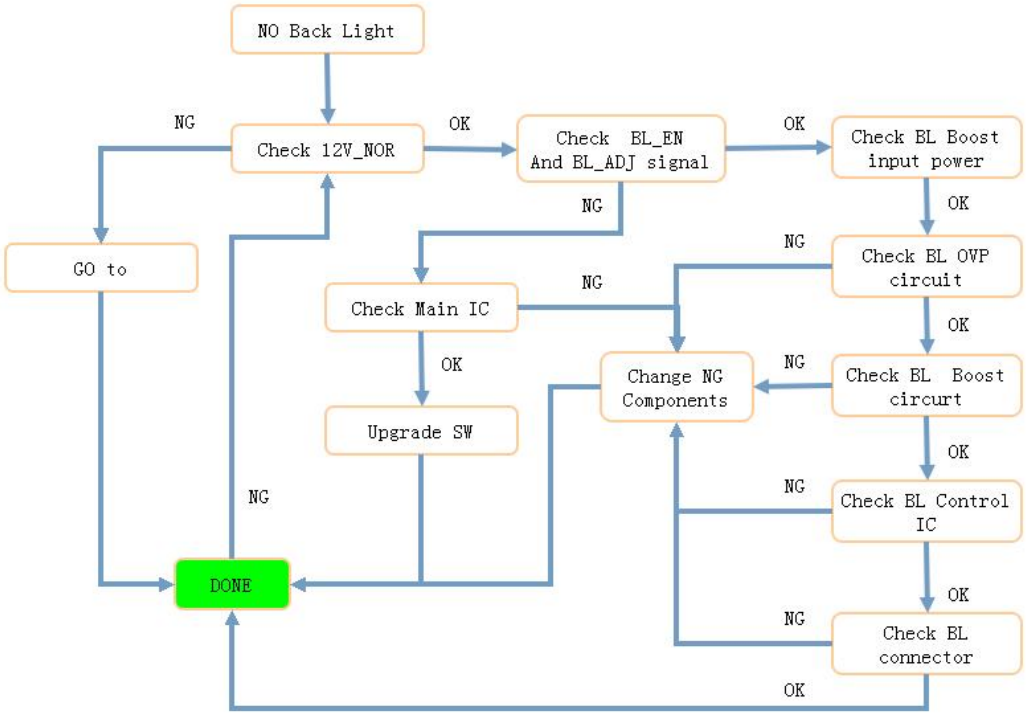
10.2 Has BackLight but no Image



10.3 Has Video but no Sound



10.4 Has Main power but no BackLight（三合一板需要，由电源设计师编写)



10.5 No main power (12V_NOR)