SERVICE MANUAL

DK1005S

CONTENTS

1. SAFETY PREAUTIONS

1.1 GENERAL GUIDELINES

1. When servicing, observe the original lead dress. if a short circuit is found, replace all parts which have been overheated or damaged by the short circuit.

2. After servicing, see to it that all the protective devices such as insulation barrier, insulation papers shields are properly installed.

3. After servicing, make the following leakage current checks to prevent the customer from being exposed to shock hazards.

2.PREVENTION OF ELECTRO STATIC DISCHARGE(ESD)TO ELECTROSTATICALLY SENSITIVE(ES)DEVICES

Some semiconductor(solid state)devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive(ES)Devices. Examples of typical ES devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by electro static discharge(ESD).

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any ESD on your body by touching a known earth ground. Alternatively, obtain and wear a commercially availabel discharging ESD wrist strap, which should be removed for potential shock reasons prior to applying power to the unit under test.

2. After removing an electrical assembly equipped with ES devices,place the assembly on a conductive surface such as alminum foil, to prevent electrostatic charge buildup or exposure of the assembly.

3. Use only a grounded-tip soldering iron to solder or unsolder ES devices.

4. Use only an anti-static solder removal device. Some solder removal devices not classified as anti-static (ESD protected)can generate electrical charge sufficient to damage ES devices.

5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ES devices.

6. Do not remove a replacement ES device from its protective package until immediately before you are ready to install it. (Most replacement ES devices are packaged with leads electrically shorted together by conductive foam, alminum foil or comparable conductive material).

7. Immediately before removing the protective material from the leads of a replacement ES device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

Caution

Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

8. Minimize bodily motions when handling unpackaged replacement ES devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity(ESD).

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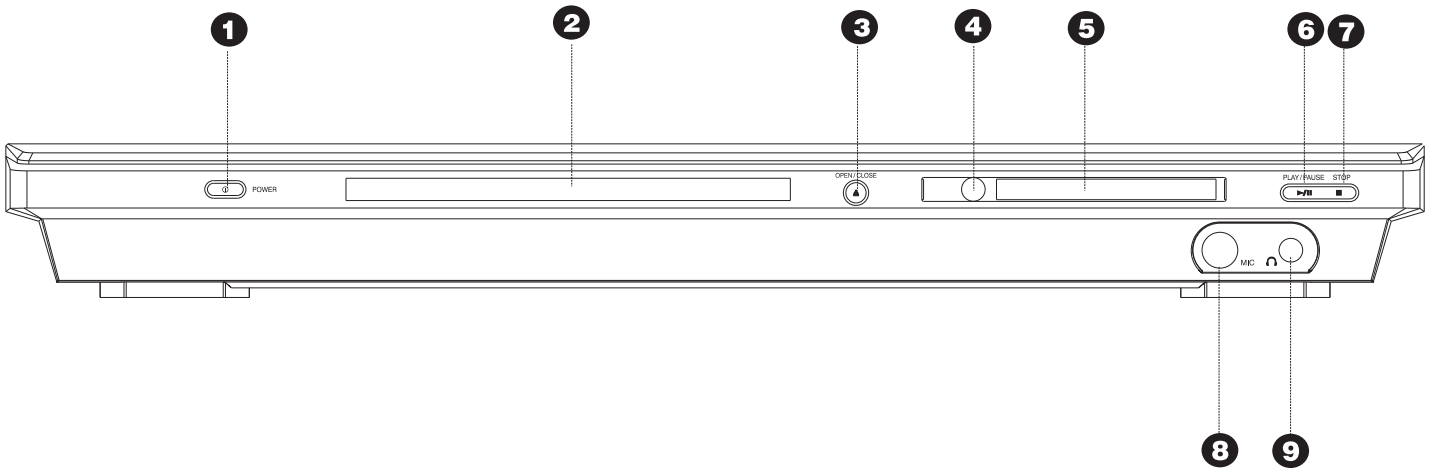
IMPORTANT SAFETY NOTICE

There are special components used in this equipment which are imporant for safety.
These parts are marked by ⚠ in the schematic diagrams, Exploded Views and replacement parts list. It is essential that these critical parts should be replaced with manufacturer's specified parts to prevent shock, fire, or other hazards. Do not modify the original design without permission of manufacturer.

▪ Front Panel Illustration



❶ POWER switch

❷ Disc tray

❸ OPEN/CLOSE button

❹ Remote control signal sensor

❺ LED display window

❻ PLAY/PAUSE button

❼ STOP button

❽ MIC jack

❾ Headphone jack

4.PREVENTION OF STATIC ELECTRICITY DISCHARGE

The laser diode in the traverse unit (optical pickup)may brake down due to static electricity of clothes or human body. Use due caution to electrostatic breakdown when servicing and handling the laser diode.

4.1.Grounding for electrostatic breakdown prevention

Some devices such as the DVD player use the optical pickup(laser diode)and the optical pickup will be damaged by static electricity in the working environment.Proceed servicing works under the working environment where grounding works is completed.

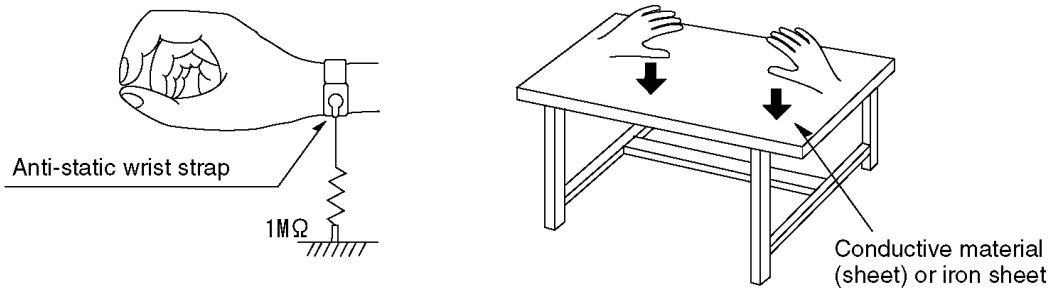
4.1.1. Worktable grounding

1. Put a conductive material(sheet)or iron sheet on the area where the optical pickup is placed,and ground the sheet.

4.1.2.Human body grounding

1 Use the anti-static wrist strap to discharge the static electricity from your body.

safety_3 (1577x409x2 tiff)



4.1.3.Handling of optical pickup

1. To keep the good quality of the optical pickup maintenance parts during transportation and before installation, the both ends of the laser diode are short-circuited.After replacing the parts with new ones, remove the short circuit according to the correct procedure. (See this Technical Guide).

2. Do not use a tester to check the laser diode for the optical pickup .Failure to do so willdamage the laser diode due to the power supply in the tester.

4.2. Handling precautions for Traverse Unit (Optical Pickup)

1. Do not give a considerable shock to the traverse unit(optical pickup)as it has an extremely high-precise structure.

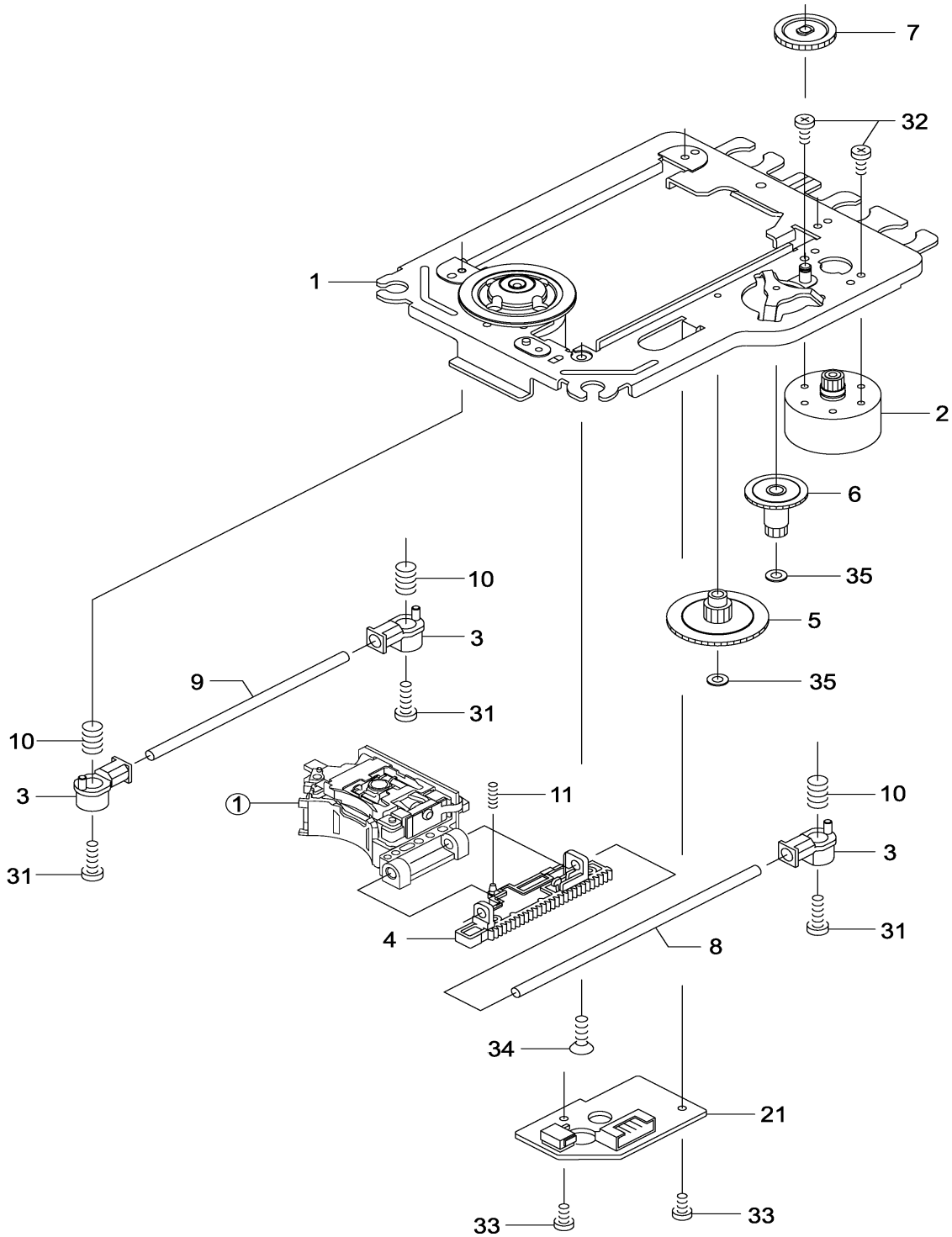
2. When replacing the optical pickup, install the flexible cable and cut is short land with a nipper. See the optical pickup replacement procedure in this Technical Guide. Before replacing the traverse unit, remove the short pin for preventingstatic electricity and install a new unit.Connect the connector as short times as possible.

3. The flexible cable may be cut off if an excessive force is applied to it.Use caution when handling the cable

4. The half-fixed resistor for laser power adjustment cannot be adjusted. Do not turn the resistor.

5. Assembling and disassembling the mechanism unit

5.1 Optical pickup Unit Explosed View and Part List



Pic (1)

Materials to Pic (1)

No.	PARTS CODE	PARTS NAME	Q'ty
①	14692200	SF-HD60	1
1	1EA0311A06300	ASSY, CHASSIS, COMPLETE	1
2	1EA0M10A15500	ASSY, MOTOR, SLED	1
Or	1EA0M10A15501	ASSY, MOTOR, SLED	1
3	1EA2451A24700	HOLDER, SHAFT	3
4	1EA2511A29100	GEAR, RACK	1
5	1EA2511A29200	GEAR, DRIVE	1
6	1EA2511A29300	GEAR, MIDDLE, A	1
7	1EA2511A29400	GEAR, MIDDLE, B	1
8	1EA2744A03000	SHAFT, SLIDE	1
9	1EA2744A03100	SHAFT, SLIDE, SUB	1
10	1EA2812A15300	SPRING, COMP, TYOUSEI	3
11	1EA2812A15400	SPRING, COMP, RACK	1
21	1EA0B10B20100	ASSY, PWB	1
Or	1EA0B10B20200	ASSY, PWB	1
31	SEXEA25700---	SPECIAL SCREW BIN+-M2X11	3
32	SEXEA25900---	SPECIAL SCREW M1.7X2.2	2
33	SFBPN204R0SE-	SCR S-TPG PAN 2X4	2
34	SFSFN266R0SE-	SCR S-TPG FLT 2.6X6	1
35	SWXEA15400---	SPECIAL WASHER 1.8X4 X0.25	2

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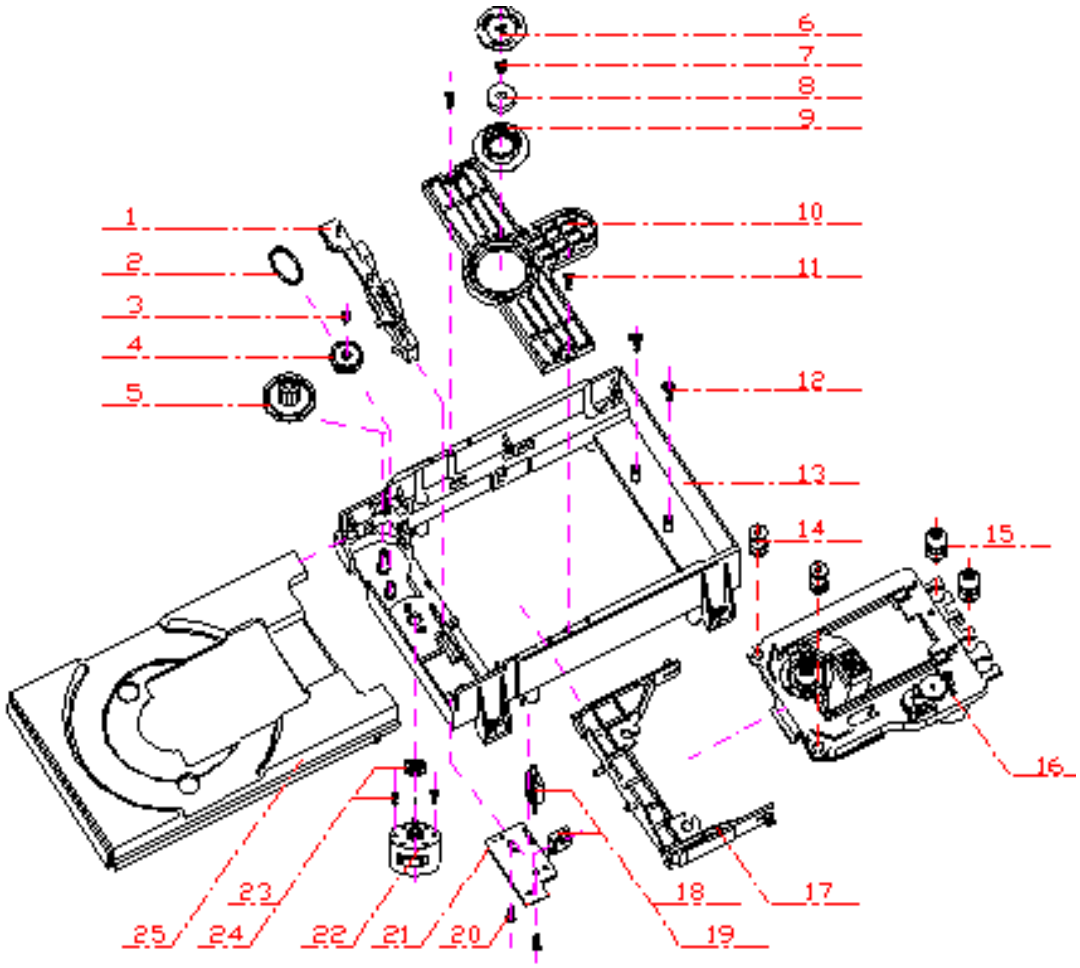
Note : This parts list is not for service parts supply.

5.2 Bracket Explosed View and Part List



Pic (2)

Materials to Pic(2)

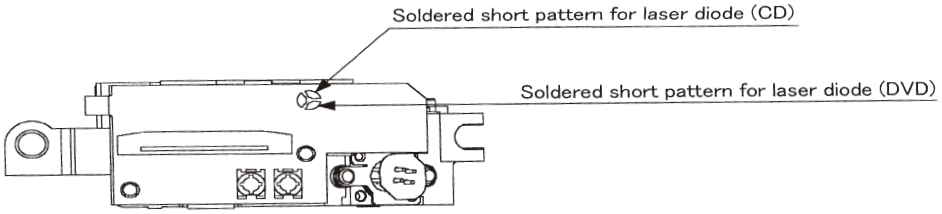
1.bracket
2.belt
3.screw
4.belt wheel
5.gearwheel
6.iron chip
7. Immobility mechanism equipment
8. Magnet
9. Platen
10. Bridge bracket
11. screw
12. screw
13. Big bracket
14. front silicon rubber
15. Back silicon rubber
16. Pick-up
17. Pick-up
18. switch
19. Five-pin flat plug
20. screw
21. PCB
22. motor
23. Motor wheel
24. screw
25.tray

Before going process with disassembly and installation, please carefully both peruse the chart and confirm the materials.

5.3 MISCELLANEOUS

5.3.1 Protection of the LD(Laser diode)

Short the parts of LD circuit pattern by soldering.



5.3.2 Cautions on assembly and adjustment

Make sure that the workbenches,jigs,tips,tips of soldering irons and measuring instruments are grounded,and that personnel wear wrist straps for ground.

Open the LD short lands quickly with a soldering iron after a circuit is connected.

Keep the power source of the pick-up protected from internal and external sources of electrical noise.

Refrain from operation and storage in atmospheres containing corrosive gases (such as H2S,SO2, NO2 and Cl2)or toxic gases or in locations containing substances(especially from the organic silicon,cyan, formalin and phenol groups)which emit toxic gases.It is particularly important to ensure that none of the above substances are present inside the unit.Otherwise,the motor may no longer run.

6.Electrical Confirmation

6.1. Video Output (Luminance Signal) Confirmation

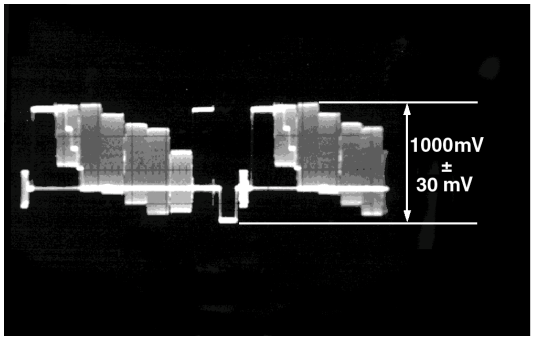
DO this confirmation after replacing a P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
200mV/dir,10 μ sec/dir	1000mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

1.Connect the oscilloscope to the video output terminal and terminate at 75 ohms.

2.Confirm that luminance signal(Y+S)level is 1000mVp-p±30mV



6.2 Video Output(Chrominance Signal) Confirmation

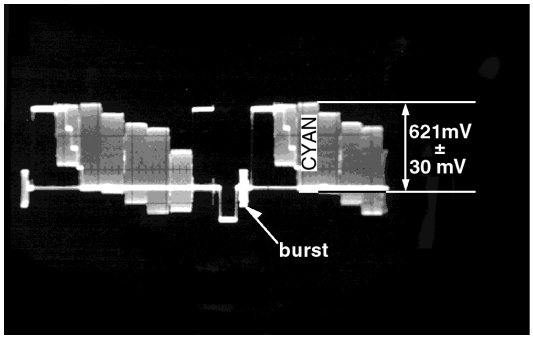
Do the confirmation after replacing P.C.B.

Measurement point	Mode	Disc
Video output terminal	Color bar 75% PLAY(Title 46):DVDT-S15 PLAY(Title 12):DVDT-S01	DVDT-S15 or DVDT-S01
Measuring equipment,tools	Confirmation value	
Screwdriver,Oscilloscope 200mV/dir,10 μ sec/dir	621mVp-p±30mV	

Purpose:To maintain video signal output compatibility.

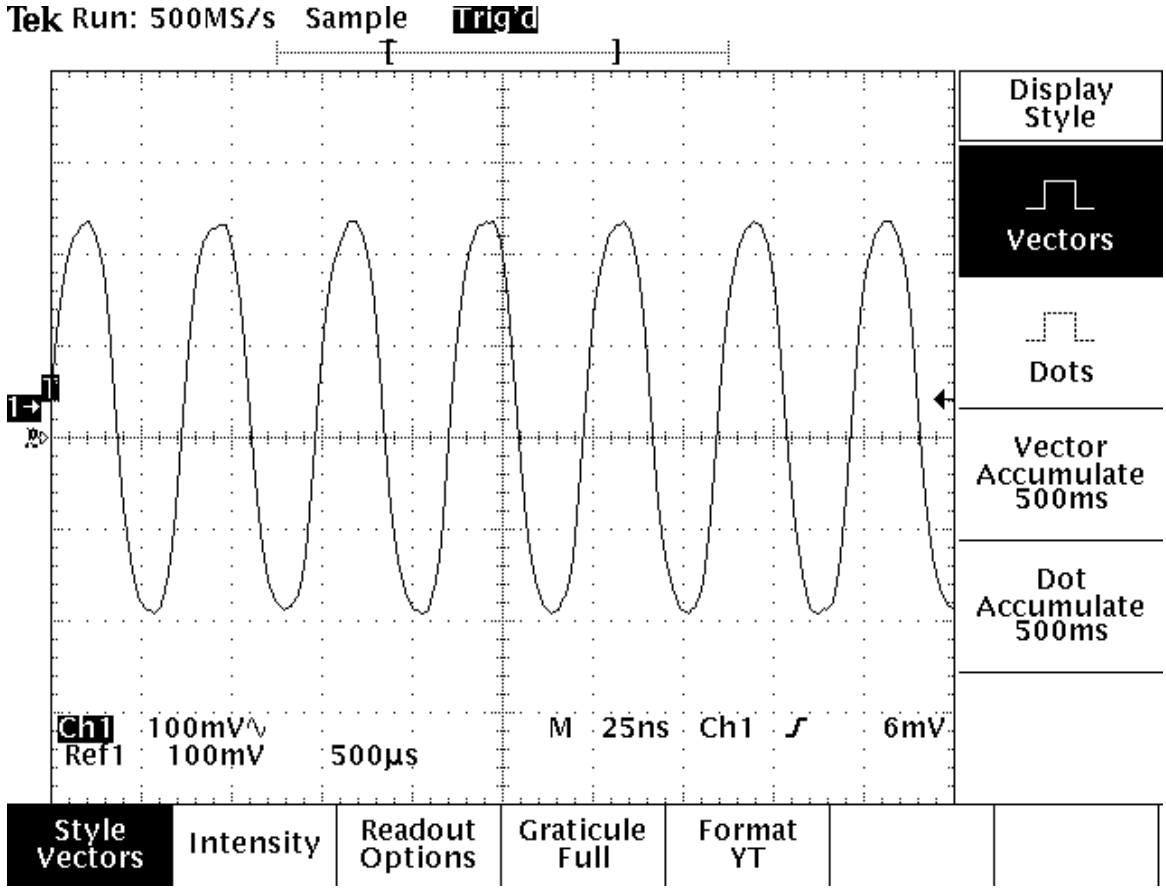
1.Connect the oscilloscope to the video output terminal and terminate at 75 ohme.

2.Confirm that the chrominance signal(C)level is 621 mVp-p±30mV

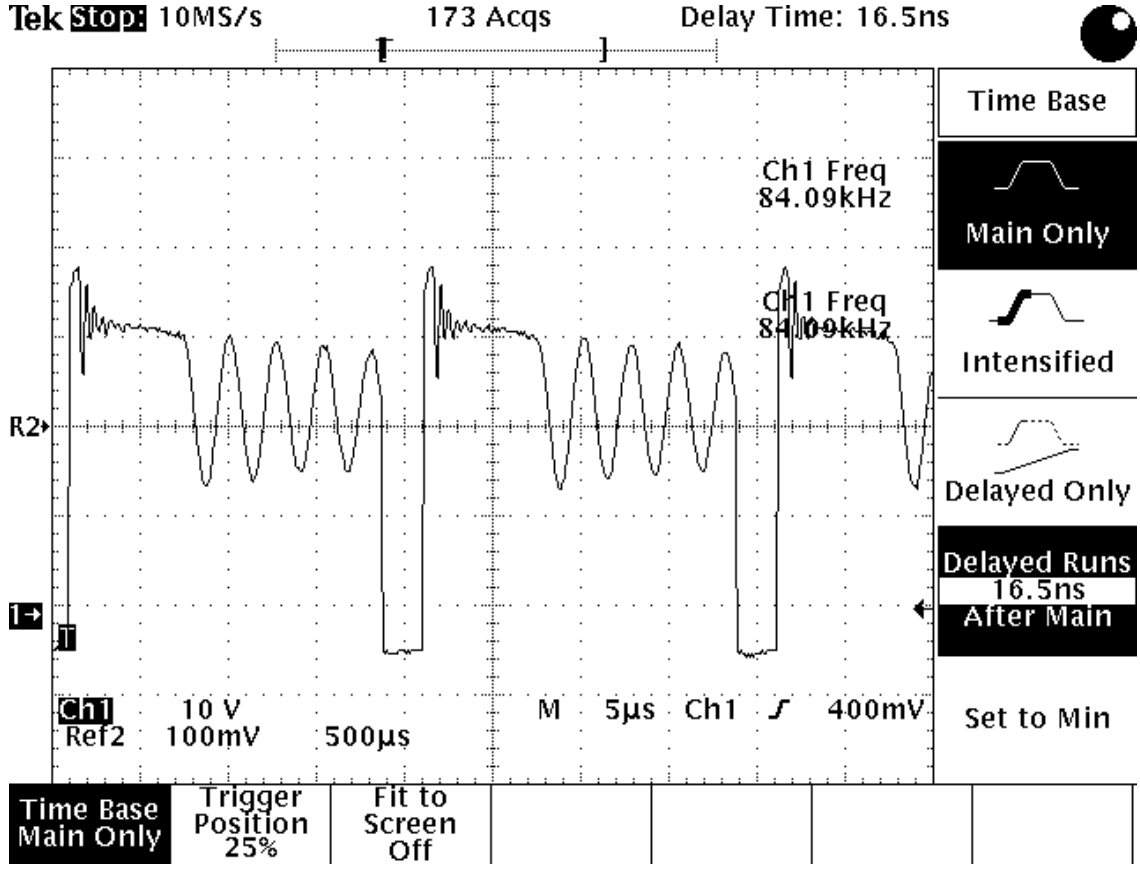


7.MPEG BOARD CHECK WAVEFORM

7.1 27MHz WAVEFORM



7.2 IC5L0380R PIN.2 WAVEFORM DIAGRAM



16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.23 µm process technology**
  - — Fully compatible with 0.32 µm Am29LV160B device
- **High performance**
  - — Access times as fast as 70 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 9 mA read current
  - — 20 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-system or via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **20-year data retention at 125°C**
  - — Reliable operation for the life of the system
- **Package option**
  - — 48-ball FBGA
  - — 48-pin TSOP
  - — 44-pin SO
- **CFI (Common Flash Interface) compliant**
  - — Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion (not available on 44-pin SO)
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

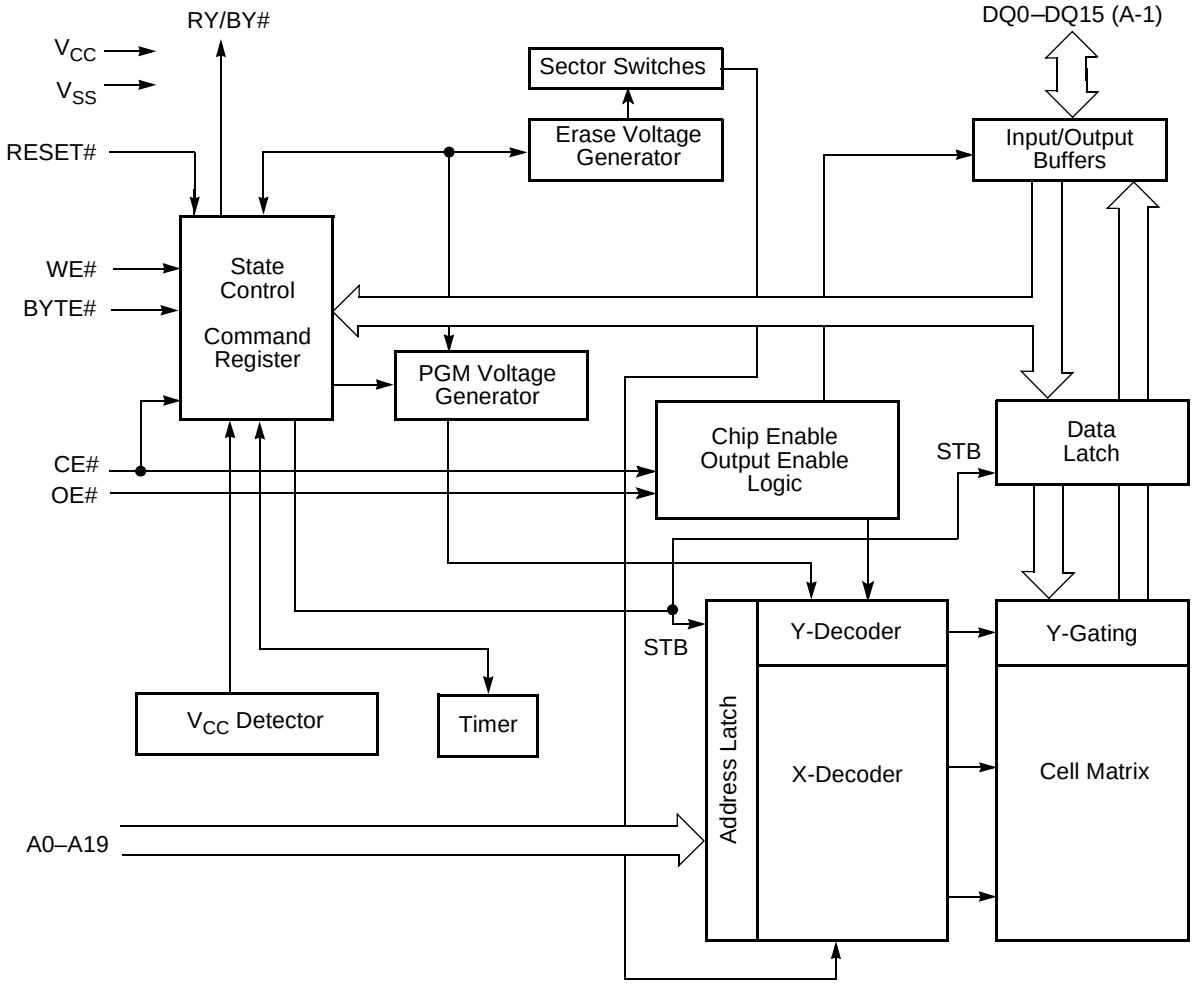
Publication# **22358** Rev: **B** Amendment/**+3**
Issue Date: **November 10, 2000**

PRODUCT SELECTOR GUIDE

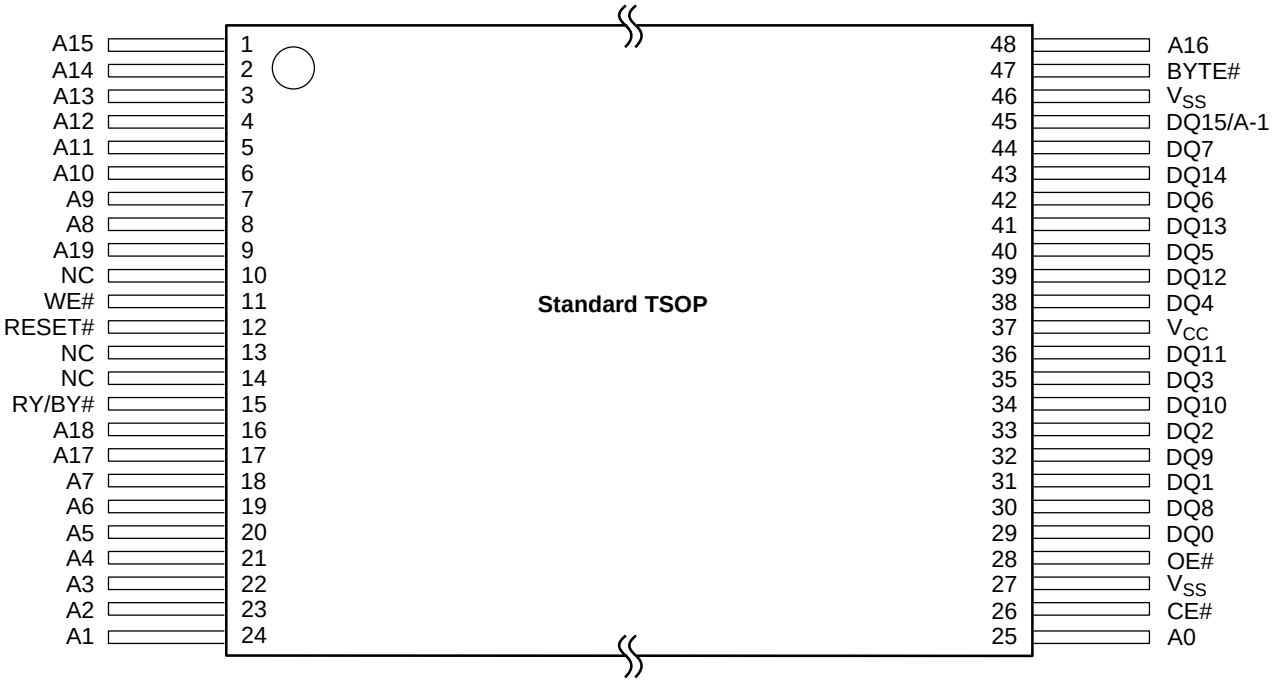
Family Part Number		Am29LV160D		
Speed Option	Voltage Range: V_{CC} = 2.7–3.6 V	**-70**	**-90**	**-120**
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

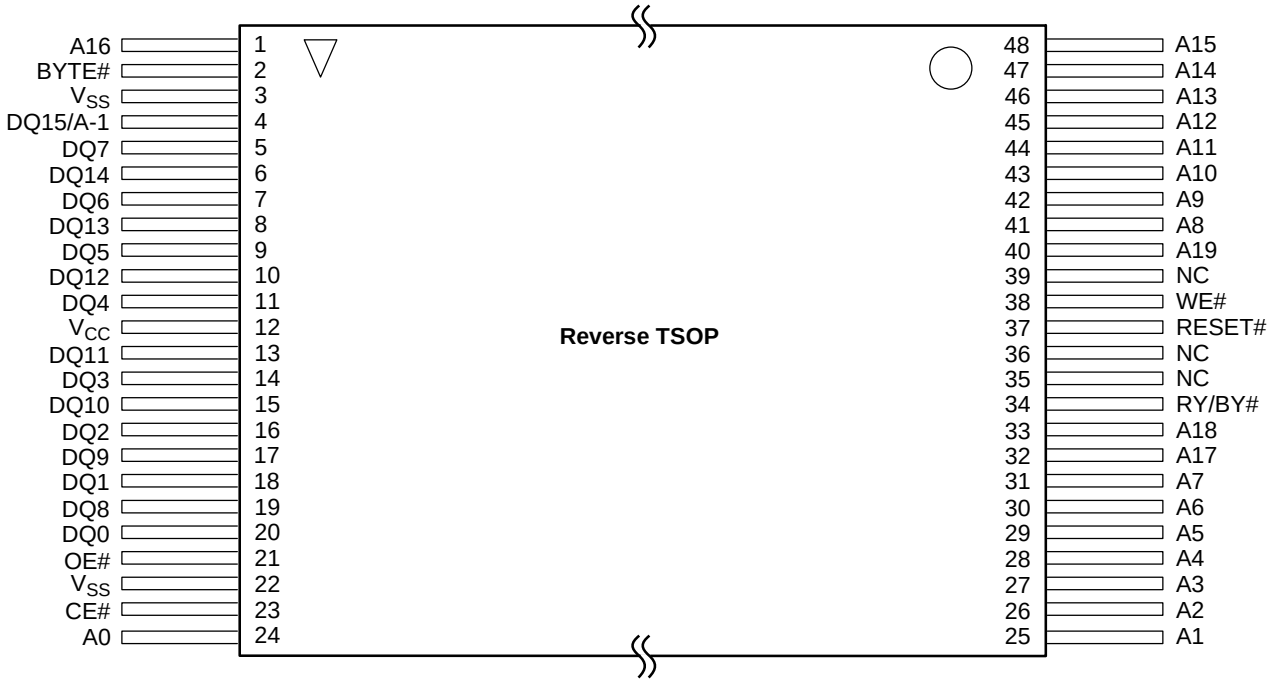
Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM

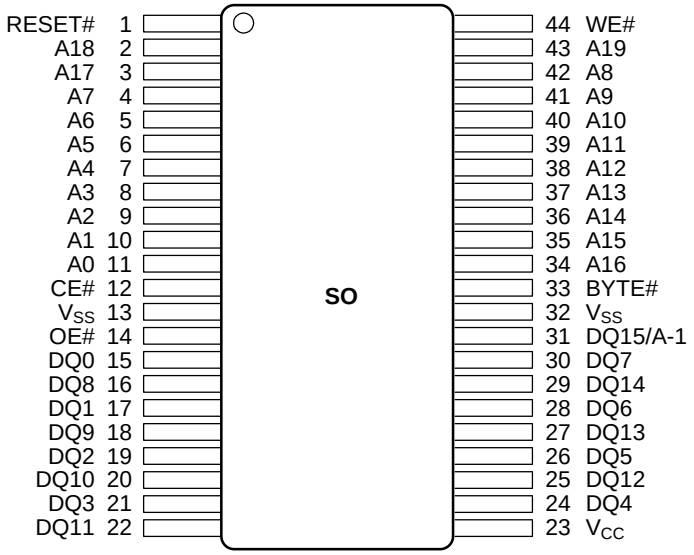


CONNECTION DIAGRAMS





CONNECTION DIAGRAMS



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	A19	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions

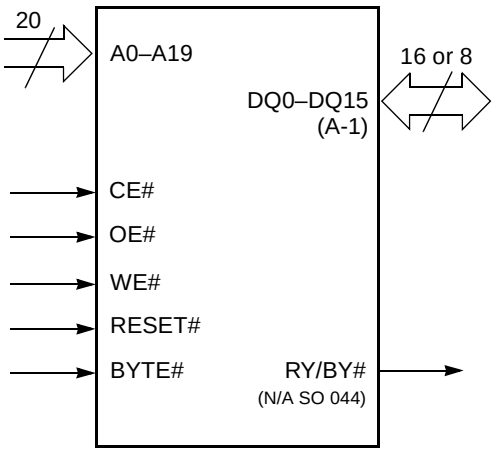
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A19	=	20 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin
RY/BY#	=	Ready/Busy output (N/A SO 044)
V_{CC}	=	3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



8.1 HY57V641620HG

DESCRIPTION

The Hyundai HY57V641620HG is a 67,108,864-bit CMOS Synchronous DRAM, ideally suited for the main memory applications which require large memory density and high bandwidth. HY57V641620HG is organized as 4banks of 1,048,576x16.

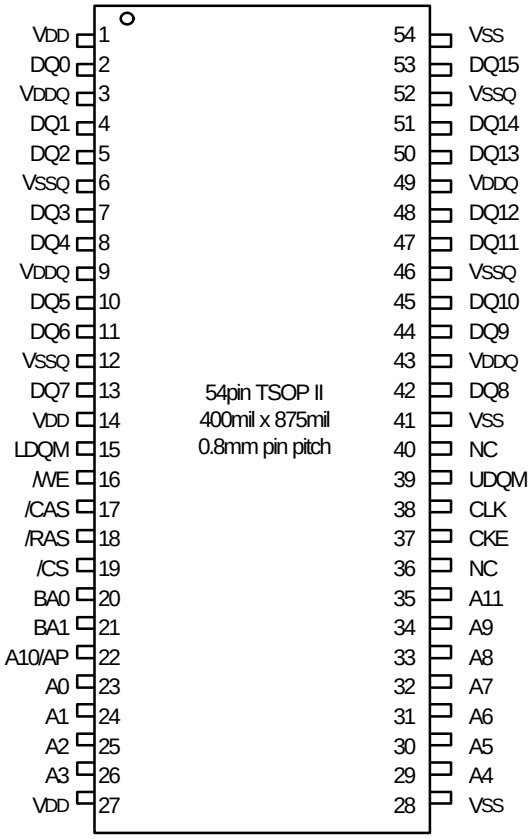
HY57V641620HG is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or Full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- Single 3.3±0.3V power supply Note)
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 54pin TSOP-II with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM or LDQM
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or Full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks

PIN CONFIGURATION

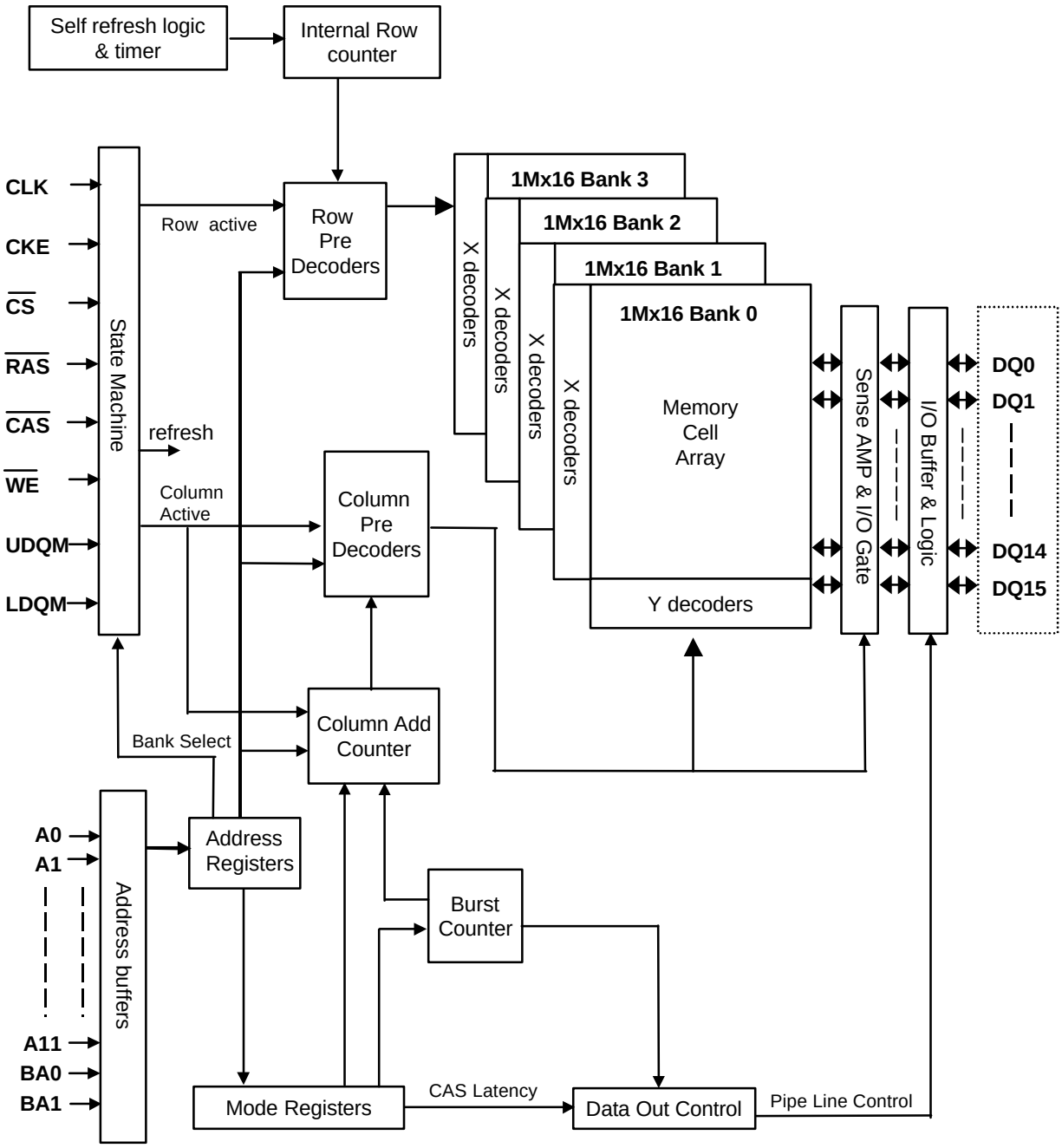


PIN DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
VDD/VSS	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

FUNCTIONAL BLOCK DIAGRAM

1Mbit x 4banks x 16 I/O Synchronous DRAM



MT1389

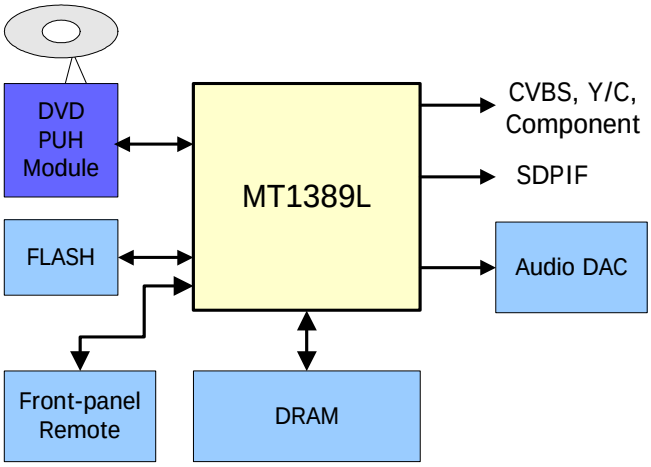
Progressive-Scan DVD Player SOC

Specifications are subject to change without notice

MediaTek MT1389 is a DVD player system-on-chip (SOC) which incorporates advanced features like high quality TV encoder and state-of-art de-interlace processing. The MT1389 enables consumer electronics manufacturers to build high quality, cost-effective DVD players, portable DVD players or any other home entertainment audio/video devices.

Based on MediaTek's world-leading DVD player SOC architecture, the MT1389 is the 3rd generation of the DVD player SOC. It integrates the MediaTek 2nd generation front-end analog RF amplifier and the Servo/MPEG AV decoder.

The progressive scan of the MT1389 utilized a proprietary advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. It can easily detect 3:2/2:2 pull down source and restore the correct original pictures. It also supports a patent-pending edge-preserving algorithm to remove the saw-tooth effect.



DVD Player System Diagram Using MT1389

Key Features

- RF/Servo/MPEG Integration
- High Performance Audio Processor
- Motion-Adaptive, Edge-Preserving De-interlace
- 108MHz/12-bit, 6 CH TV Encoder

Applications

- Standard DVD Players
- Portable DVD Players

General Feature List

- Super Integration DVD player single chip
  - High performance analog RF amplifier
  - Servo controller and data channel processing
  - MPEG-1/MPEG-2/JPEG video
  - Dolby AC-3/DTS/DVD-Audio
  - Unified memory architecture
  - Versatile video scaling & quality enhancement
  - OSD & Sub-picture
  - 2-D graphic engine
  - Built-in clock generator
  - Built-in high quality TV encoder
  - Built-in progressive video processor
  - Audio effect post-processor
  - Audio input port

- High Performance Analog RF Amplifier
  - Programmable fc
  - Dual automatic laser power control
  - Defect and blank detection
  - RF level signal generator

- Speed Performance on Servo/Channel Decoding
  - DVD-ROM up to 4XS
  - CD-ROM up to 24XS

- Channel Data Processor
  - Digital data slicer for small jitter capability
  - Built-in high performance data PLL for channel data demodulation
  - EFM/EFM+ data demodulation
  - Enhanced channel data frame sync protection & DVD-ROM sector sync protection

- Servo Control and Spindle Motor Control
  - Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
  - Built-in ADCs and DACs for digital servo control
  - Provide 2 general PWM
  - Tray control can be PWM output or digital output

- Embedded Micro controller
  - Built-in 8032 micro controller
  - Built-in internal 373 and 8-bit programmable lower address port
  - 1024-bytes on-chip RAM
  - Up to 4M bytes FLASH-programming interface
  - Supports 5/3.3-Volt. FLASH interface
  - Supports power-down mode
  - Supports additional serial port

- DVD-ROM/CD-ROM Decoding Logic
  - High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
  - Automatic sector Mode and Form detection
  - Automatic sector Header verification
  - Decoder Error Notification Interrupt that signals various decoder errors
  - Provide error correction acceleration

- Buffer Memory Controller
  - Supports 16Mb/32Mb/64Mb/128Mb SDRAM
  - Supports 16-bit SDRAM data bus
  - Provide the self-refresh mode SDRAM
  - Block-based sector addressing
  - Support 3.3 Volt. DRAM Interface

- Video Decode
  - Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
  - Smooth digest view function with I, P and B picture decoding
  - Baseline, extended-sequential and progressive JPEG image decoding
  - Support CD-G titles

- Video/OSD/SPU/HLI Processor
  - Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
  - 65535/256/16/4/2-color bitmap format OSD,
  - 256/16 color RLC format OSD
  - Automatic scrolling of OSD image
  - Slide show transition as DVD-Audio Specification

- 2-D Graphic Engine
  - Support decode Text and Bitmap
  - Support line, rectangle and gradient fill
  - Support bitblt
  - Chroma key copy operation
  - Clip mask

- Audio Effect Processing
  - Dolby Digital (AC-3)/EX decoding
  - DTS/DTS-ES decoding
  - MLP decoding for DVD-Audio
  - MPEG-1 layer 1/layer 2 audio decoding
  - MPEG-2 layer1/layer2 2-channel audio
  - High Definition Compatible Digital (HDCD)
  - Windows Media Audio (WMA)
  - Advanced Audio Coding (AAC)
  - Dolby ProLogic II
  - Concurrent multi-channel and downmix out
  - IEC 60958/61937 output
    - PCM / bit stream / mute mode
    - Custom IEC latency up to 2 frames
  - Pink noise and white noise generator
  - Karaoke functions
    - Microphone echo
    - Microphone tone control
    - Vocal mute/vocal assistant
    - Key shift up to +/- 8 keys
    - Chorus/Flanger/Harmony/Reverb
  - Channel equalizer
  - 3D surround processing include virtual surround and speaker separation

- TV Encoder
  - Six 108MHz/12bit DACs
  - Support NTSC, PAL-BDGHINM, PAL-60
  - Support 525p, 625p progressive TV format
  - Automatically turn off unconnected channels
  - Support PC monitor (VGA)
  - Support Macrovision 7.1 L1, Macrovision 525P and 625P
  - CGMS-A/WSS
  - Closed Caption

- Progressive Output
  - Automatic detect film or video source
  - 3:2 pull down source detection
  - Advanced Motion adaptive de-interlace
  - Edge Preserving
  - Minimum external memory requirement

- Audio Input
  - Line-in/SPDIF-in for versatile audio processing

- Outline
  - 256-pin LQFP package
  - 3.3/1.8-Volt. Dual operating voltages

Data sheet acquired from Harris Semiconductor
SCHS047D

August 1998 - Revised March 2000

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The CD4051B, CD4052B, and CD4053B analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to $20V_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V_{DD}-V_{SS} = 3V, a V_{DD}-V_{EE} of up to 13V can be controlled; for V_{DD}-V_{EE} level differences above 13V, a V_{DD}-V_{SS} of at least 4.5V is required). For example, if V_{DD} = +4.5V, V_{SS} = 0V, and V_{EE} = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic “1” is present at the inhibit input terminal, all channels are off.

The CD4051B is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The CD4052B is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The CD4053B is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.

When these devices are used as demultiplexers, the “CHANNEL IN/OUT” terminals are the outputs and the “COMMON OUT/IN” terminals are the inputs.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE
CD4051BF, CD4052BF, CD4053BF	-55 to 125	16 Ld CERAMIC DIP
CD4051BE, CD4052BE, CD4053BE	-55 to 125	16 Ld PDIP
CD4051BM, CD4051BNS	-55 to 125	16 Ld SOIC
CD4051BPW, CD4052BPW, CD4053BPW	-55 to 125	16 Ld TSSOP

Features

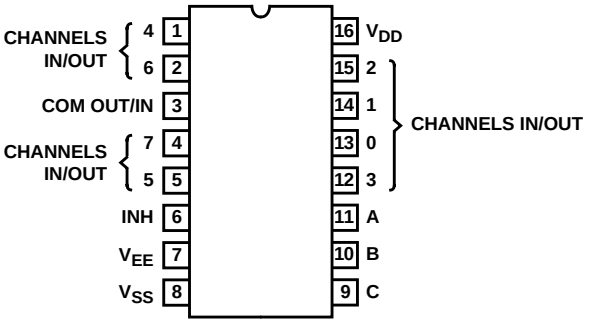
- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . . 3V to 20V
  - Analog. . . . . $\leq 20V_{P-P}$
- Low ON Resistance, 125Ω (Typ) Over $15V_{P-P}$ Signal Input Range for V_{DD}-V_{EE} = 18V
- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V_{DD}-V_{EE} = 18V
- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V_{DD}-V_{SS} = 3V to 20V) to Switch Analog Signals to $20V_{P-P}$ (V_{DD}-V_{EE} = 20V)
- Matched Switch Characteristics, r_{ON} = 5Ω (Typ) for V_{DD}-V_{EE} = 15V
- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V_{DD}-V_{SS} = V_{DD}-V_{EE} = 10V
- Binary Address Decoding on Chip
- 5V, 10V and 15V Parametric Ratings
- 10% Tested for Quiescent Current at 20V
- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25^oC
- Break-Before-Make Switching Eliminates Channel Overlap

Applications

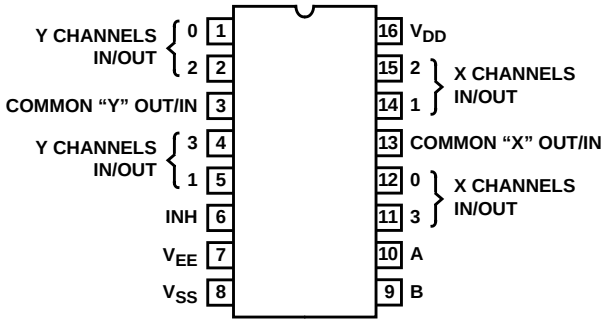
- Analog and Digital Multiplexing and Demultiplexing
- A/D and D/A Conversion
- Signal Gating

Pinouts

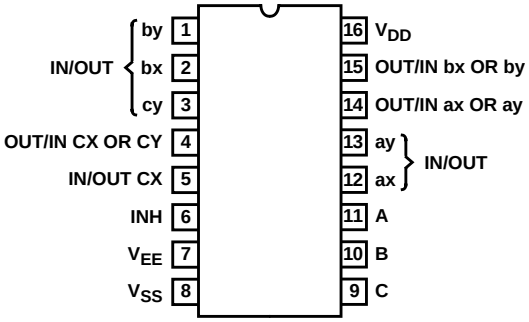
CD4051B (PDIP, CDIP, SOIC, TSSOP)
TOP VIEW



CD4052B (PDIP, CDIP, TSSOP)
TOP VIEW

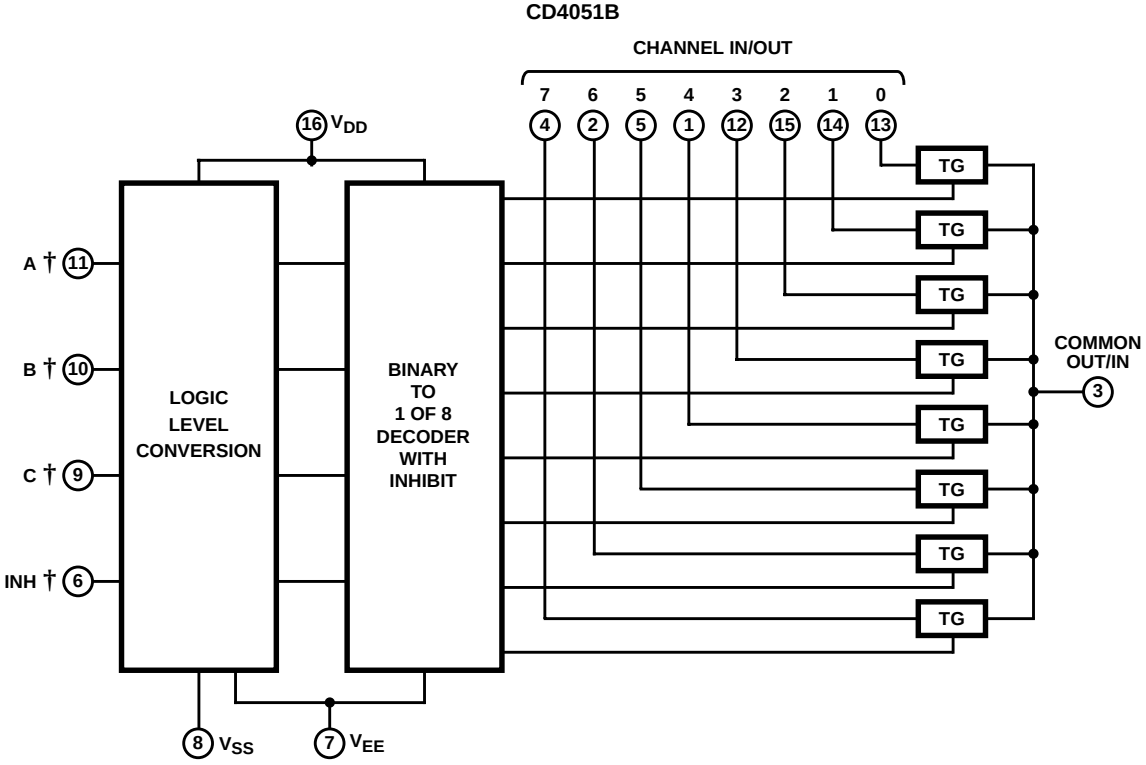


CD4053B (PDIP, CDIP, TSSOP)
TOP VIEW



Functional Block Diagrams

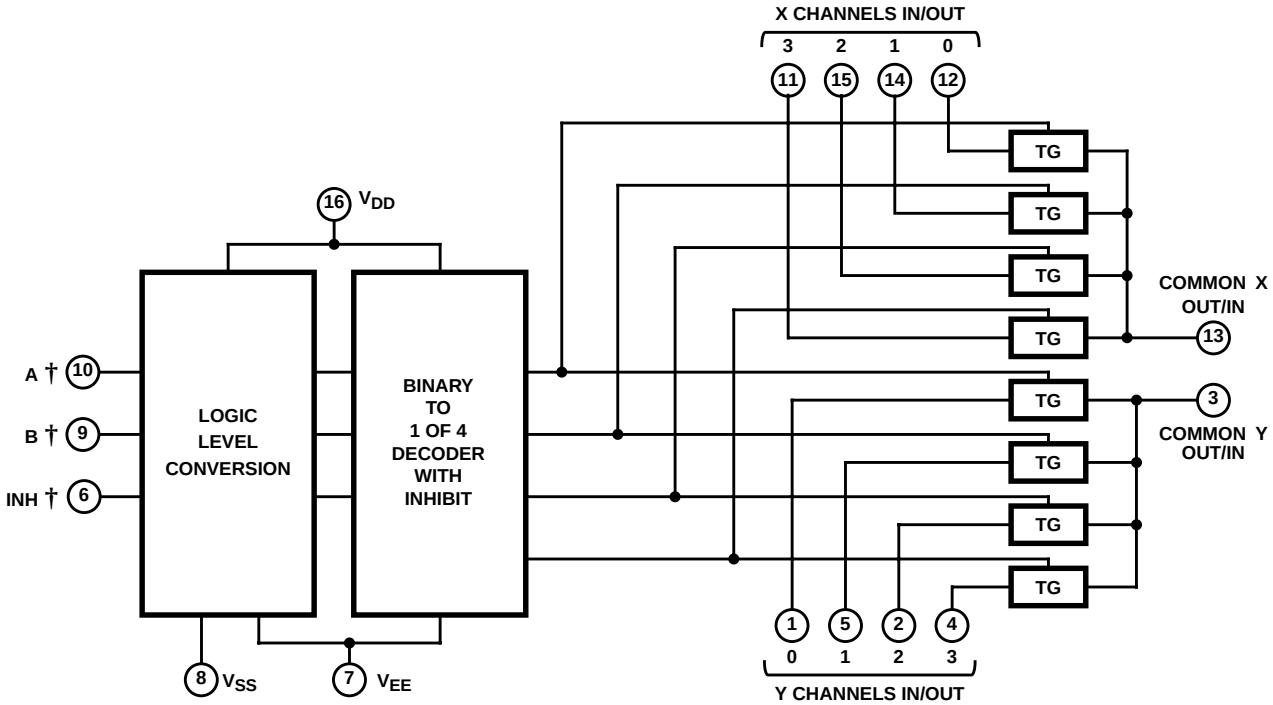
CD4051B



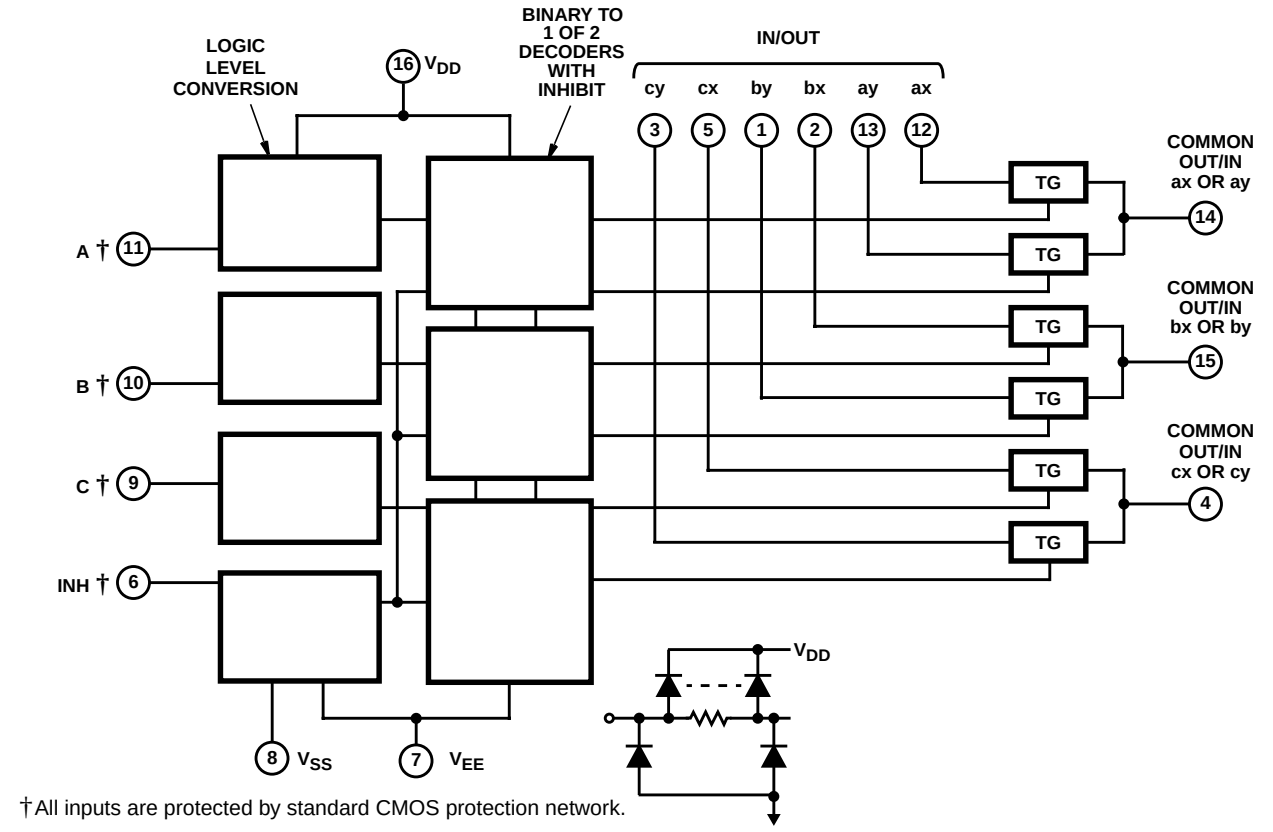
†All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

CD4052B



CD4053B



†All inputs are protected by standard CMOS protection network.

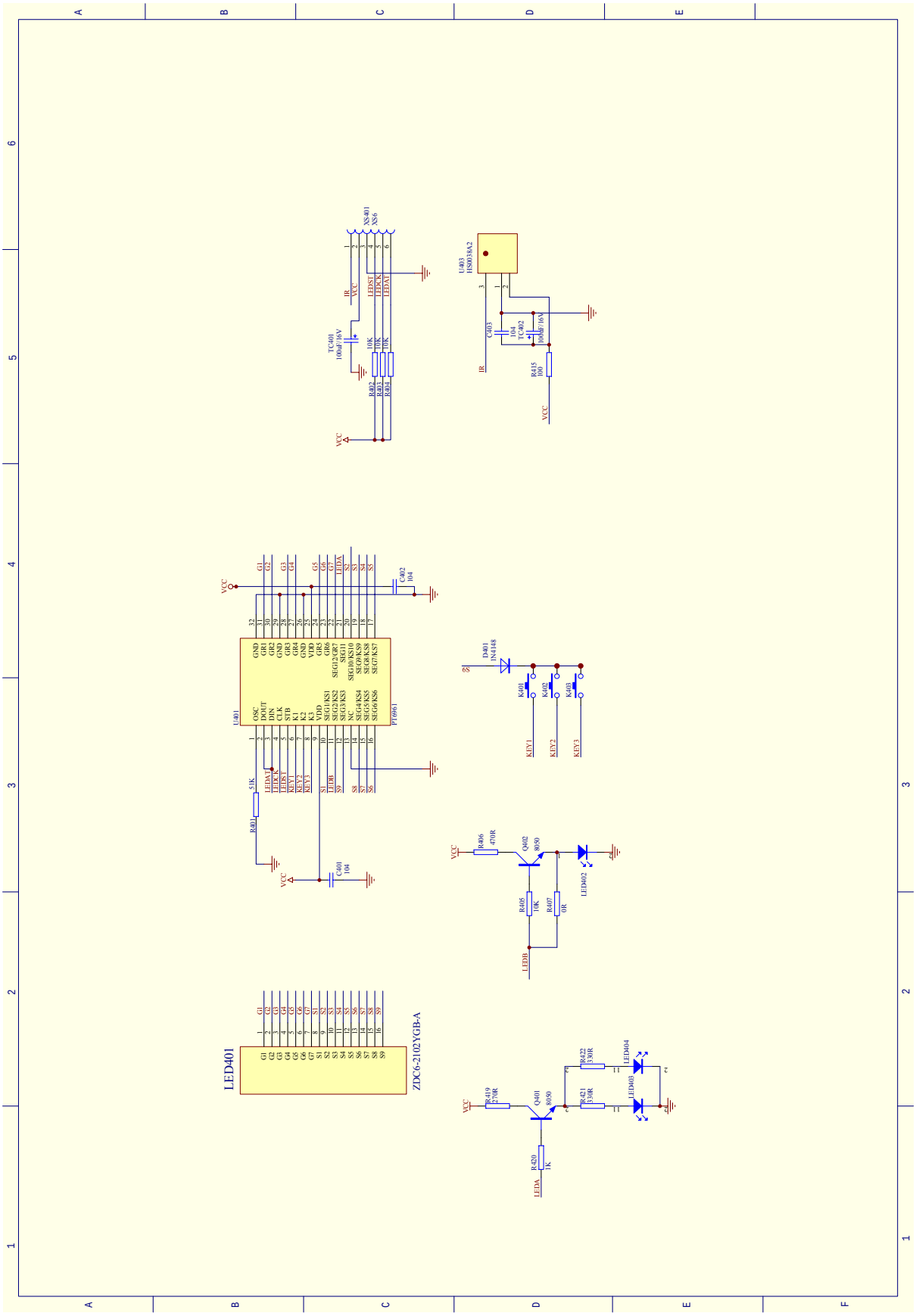
TRUTH TABLES

INPUT STATES				
INHIBIT	**C**	**B**	**A**	**“ON” CHANNEL(S)**
CD4051B				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
CD4052B				
INHIBIT	**B**		**A**	
0	0		0	0x, 0y
0	0		1	1x, 1y
0	1		0	2x, 2y
0	1		1	3x, 3y
1	X		X	None
CD4053B				
INHIBIT	**A OR B OR C**			
0	0			ax or bx or cx
0	1			ay or by or cy
1	X			None

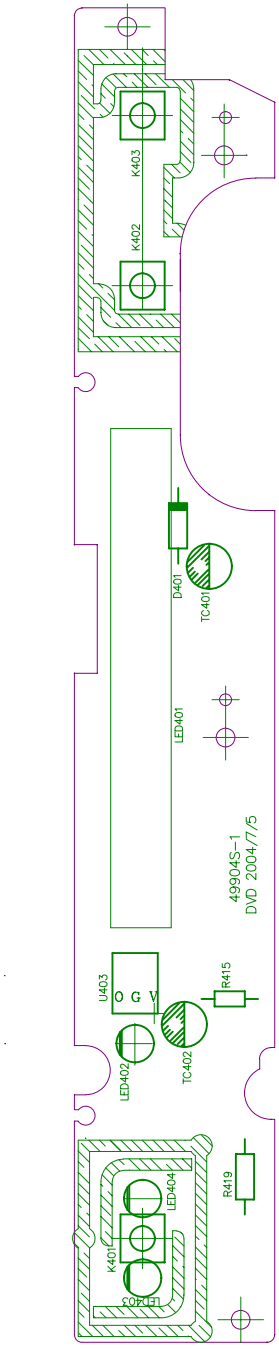
X = Don’t Care

9. SCHEMATIC & PCB WIRING DIAGRAM

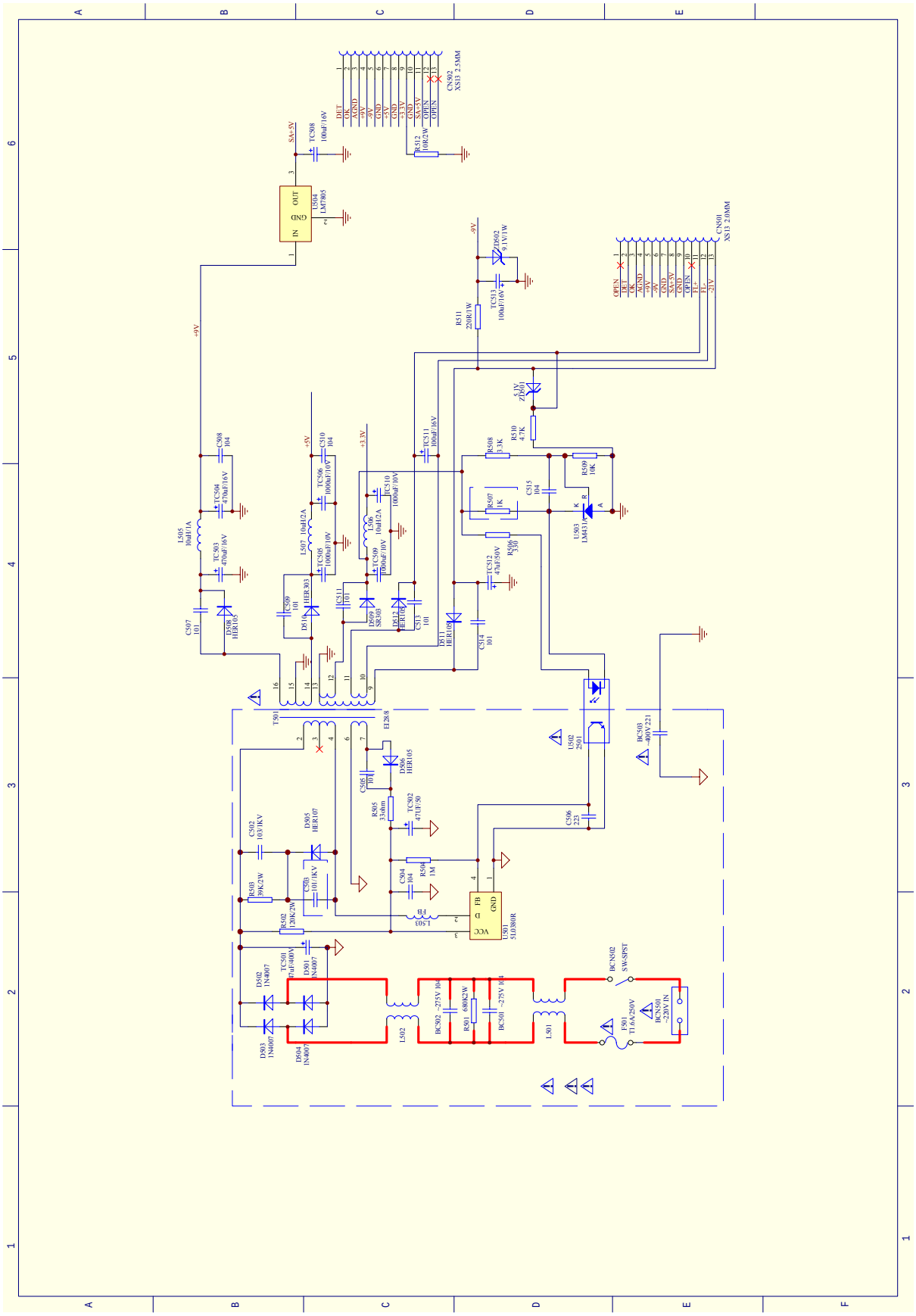
FRONT SCHEMATIC DIAGRAM



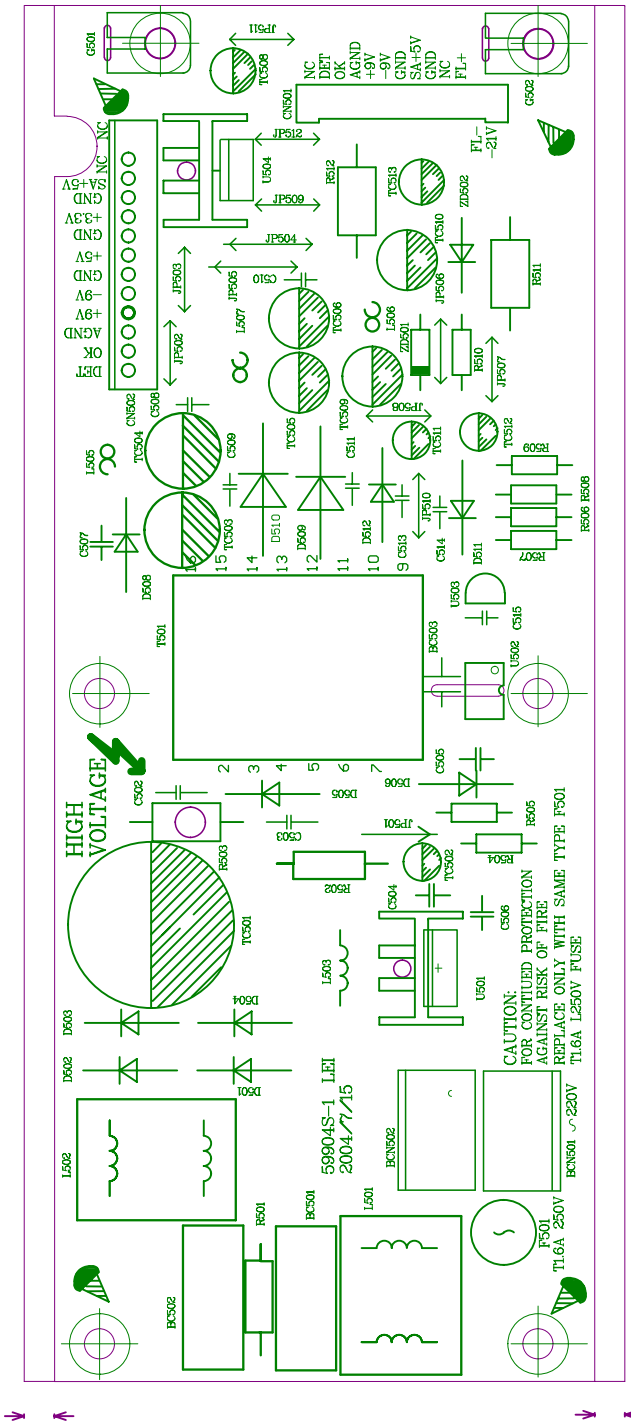
FRONT SCHEMATIC DIAGRAM



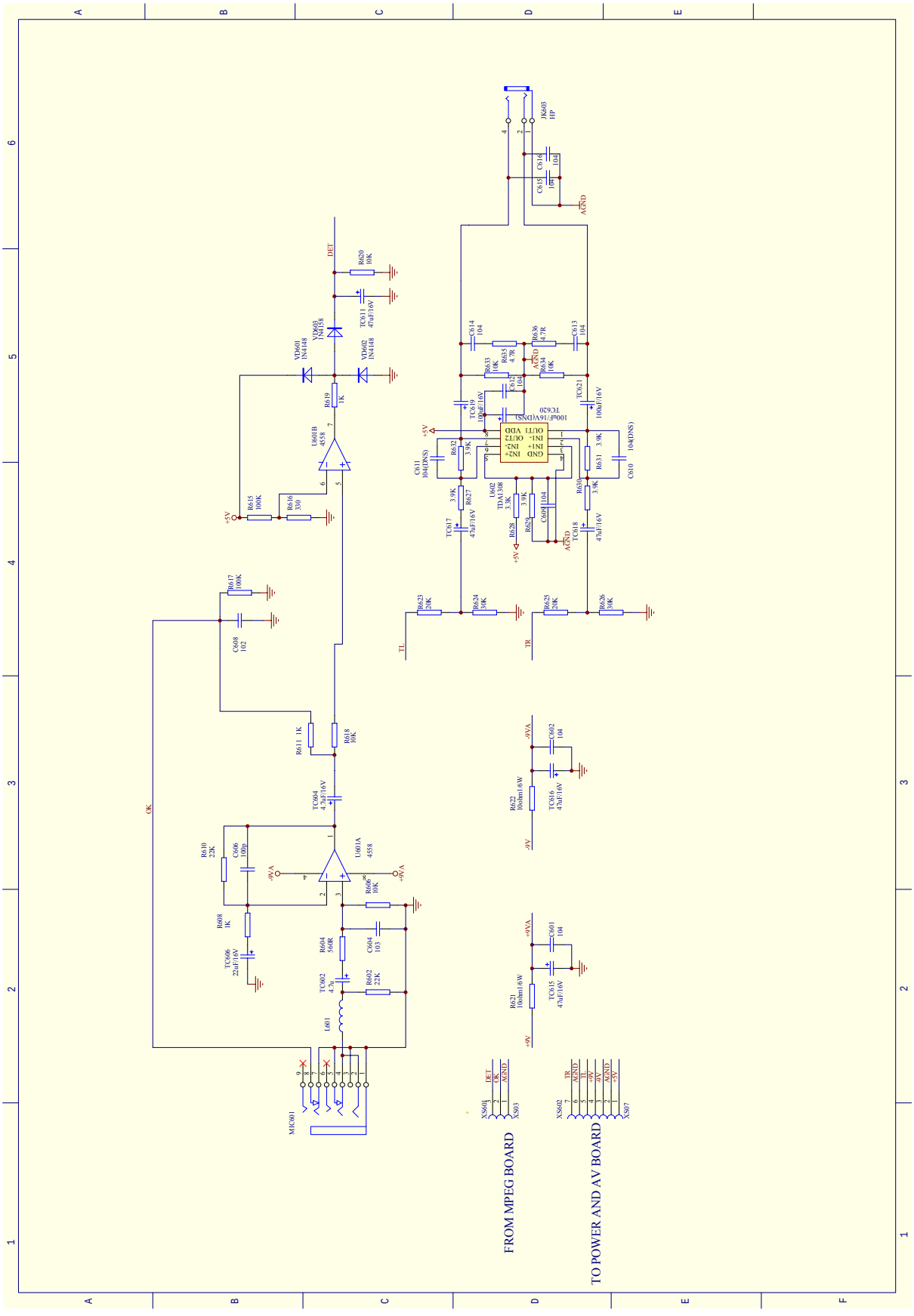
POWER BOARD SCHEMATIC DIAGRAM



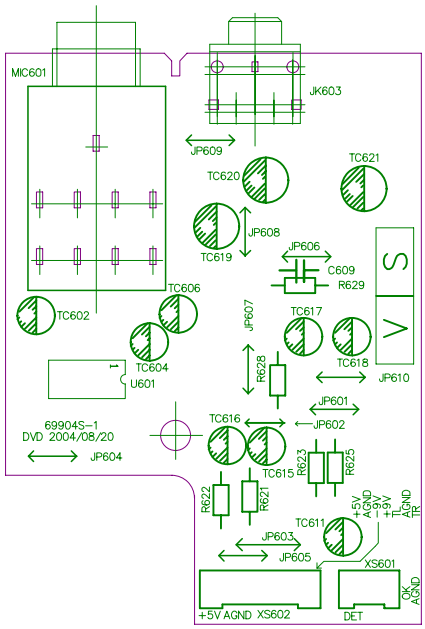
POWER BOARD SCHEMATIC DIAGRAM



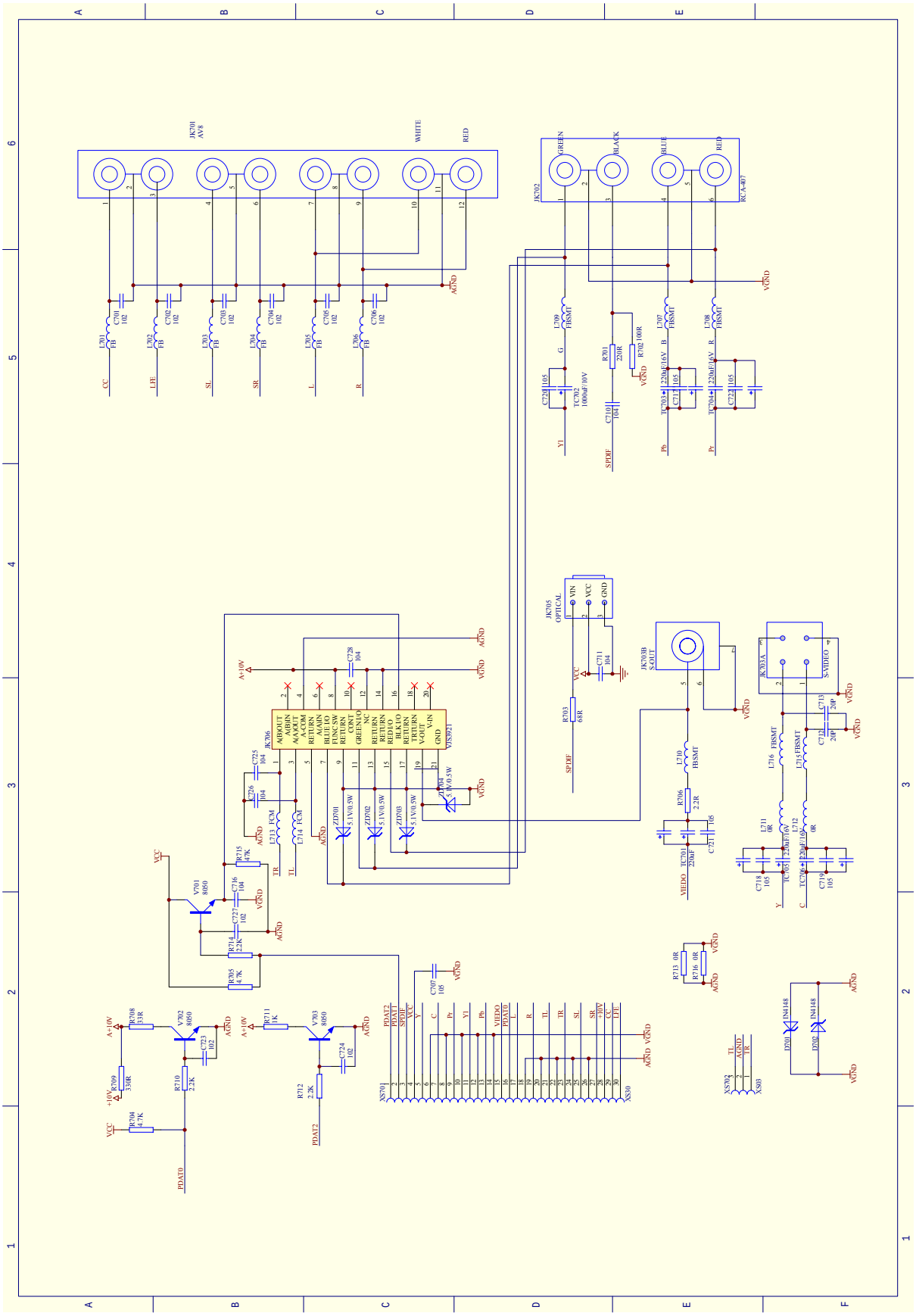
OK SCHEMATIC DIAGRAM



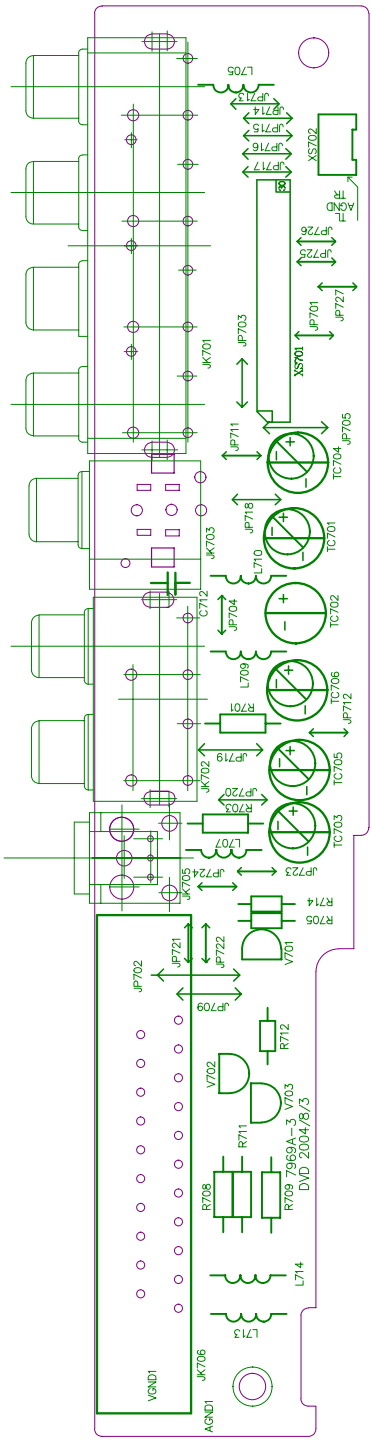
OK SCHEMATIC DIAGRAM



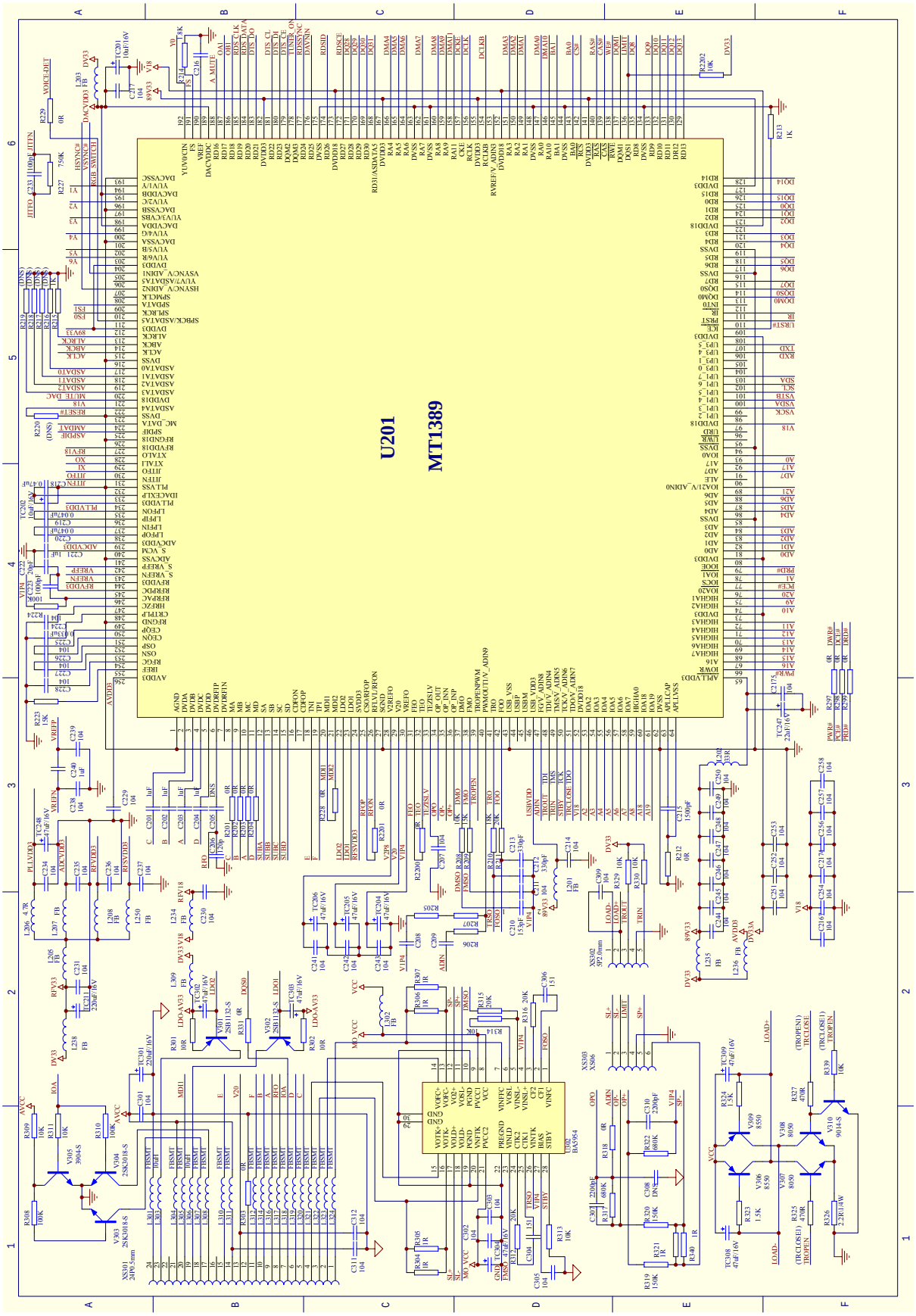
OUTPUT BOARD SCHEMATIC DIAGRAM



OUTPUT BOARD SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



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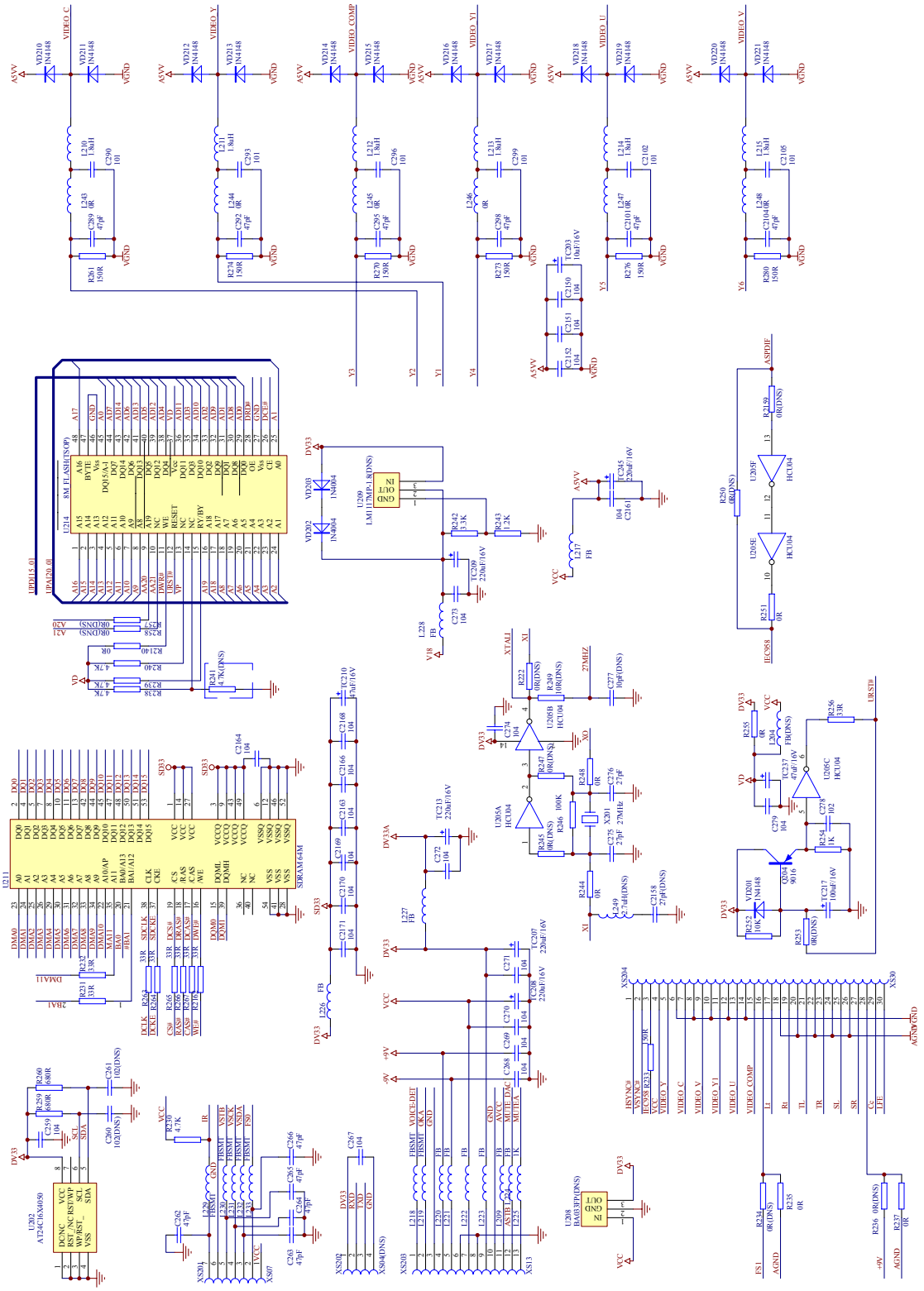
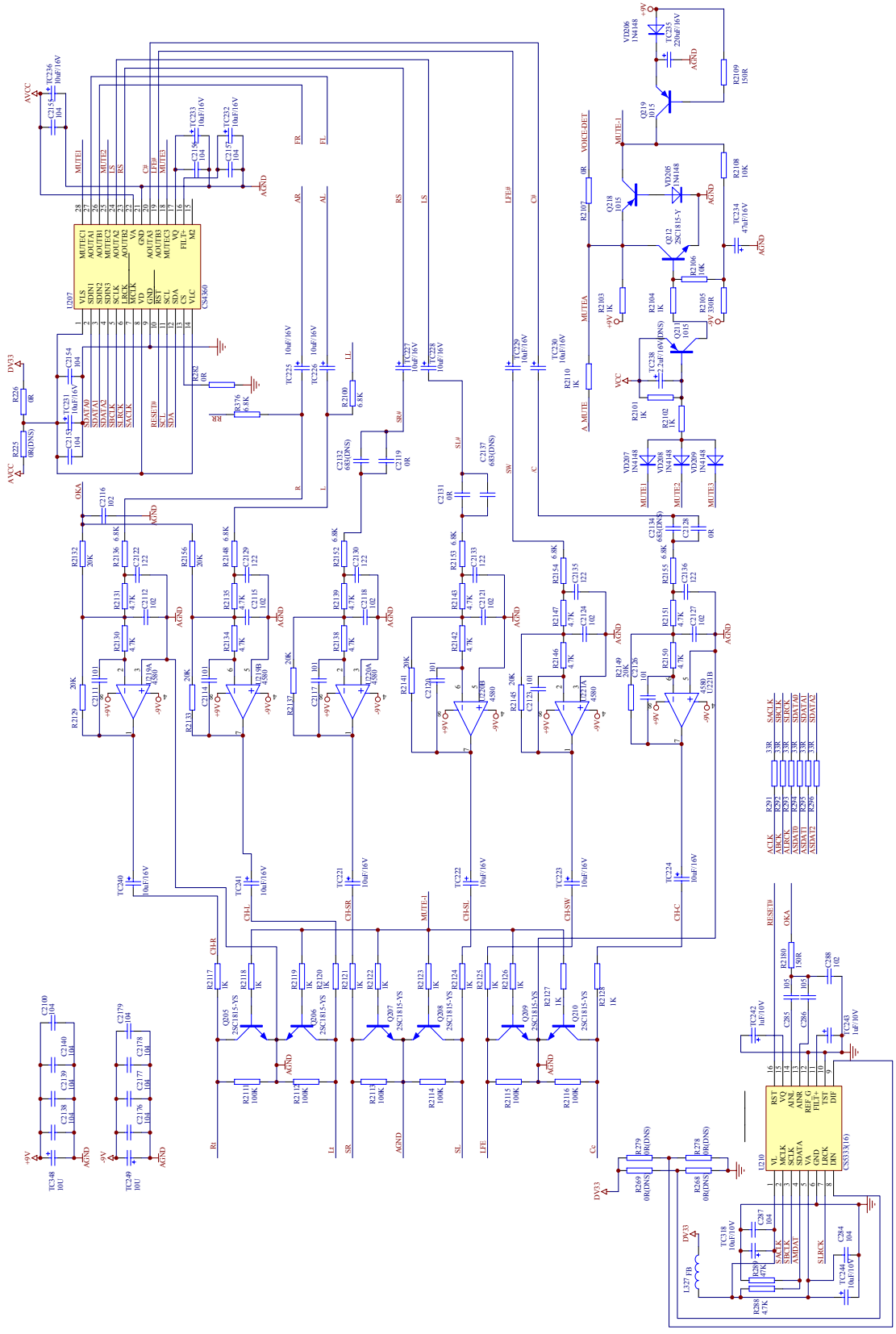
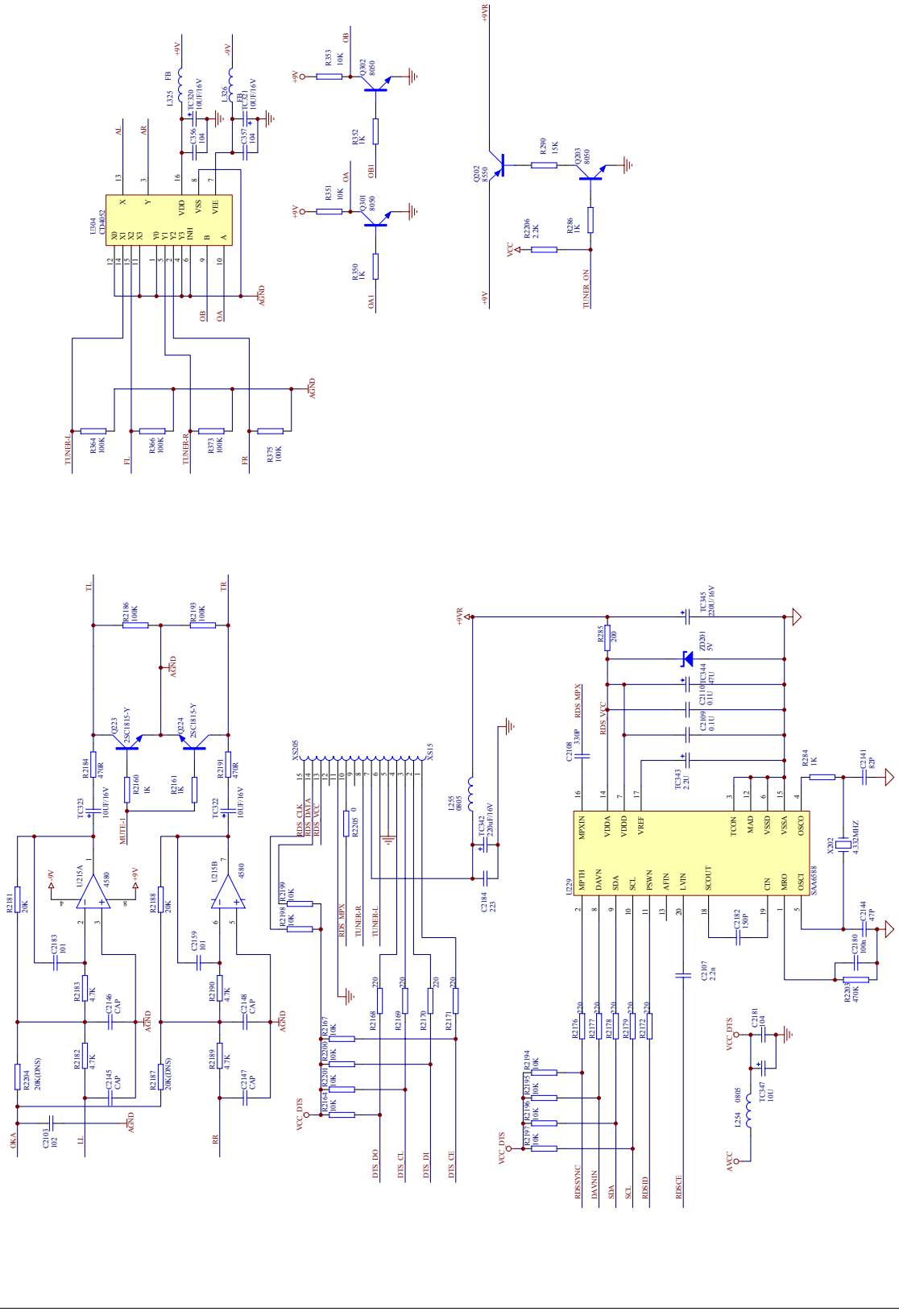


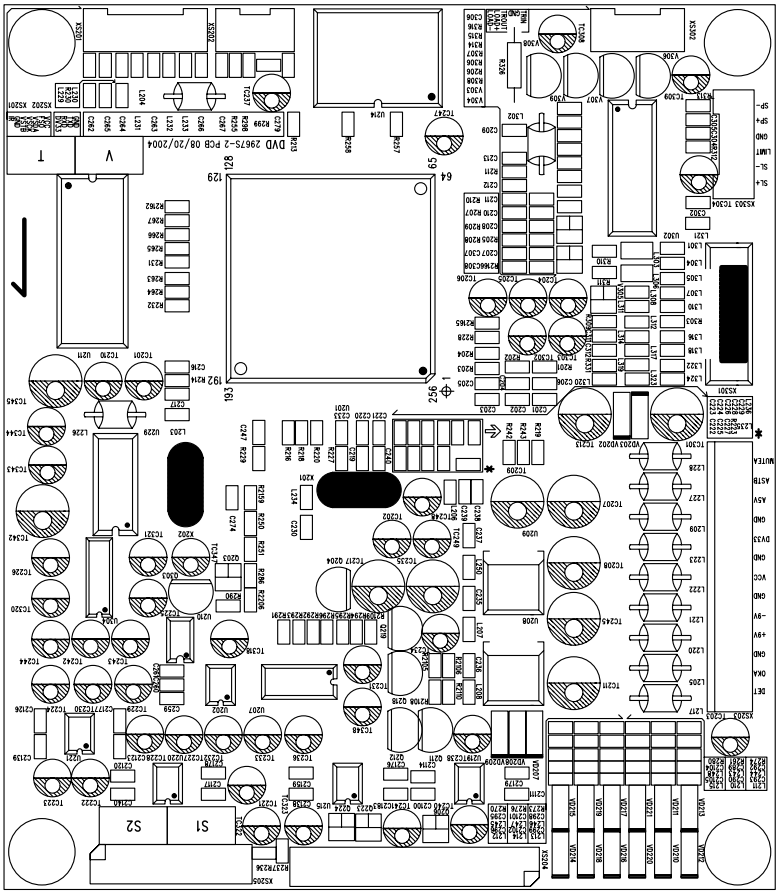
MIAN SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



MIAN SCHEMATIC DIAGRAM



10. SPARE PARTS LIST

DK1005S-2 MATERIAL LIST

1. POWER BOARD

ATERIAL COI	MATERIAL NAME	SPECIFICATIONS	UNIT	QUANTITY	LOCATION
0000273	CARBON FILM RESISTOR	1/4W33Ω±5% SHAPED 10	PCS	1	R505
0000278	CARBON FILM RESISTOR	1/4W330Ω±5% SHAPED 10	PCS	1	R506
0000294	CARBON FILM RESISTOR	1/4W10K±5% SHAPED 10	PCS	1	R507
0000289	CARBON FILM RESISTOR	1/4W4.7K±5% SHAPED 10	PCS	1	R510
0000310	CARBON FILM RESISTOR	1/4W1MΩ±5% SHAPED 10	PCS	1	R504
0010128	METAL FILM RESISTOR	1/4W 3.9K ±1% SHAPED 10	PCS	1	R508
0010101	METAL FILM RESISTOR	1/4W12K±1% SHAPED 10	PCS	1	R509
0010134	METAL OXIDE FILM RESISTOR	1W330Ω±5% SHAPED R 15×8	PCS	1	R511
0010135	METAL OXIDE FILM RESISTOR	2W39K±5% SHAPED FLAT 15×9	PCS	1	R503
0010159	METAL OXIDE FILM RESISTOR	2W39K±5% SHAPED FLAT 15×7	PCS	1	R503
0010148	METAL OXIDE FILM RESISTOR	2W120K±5% SHAPED FLAT 15×7	PCS	1	R502
0010219	METAL OXIDE FILM RESISTOR	2W10Ω±5% SHAPED FLAT 15×7	PCS	1	R512
0070001	HIGH VOLTAGE RESISTOR	1/2W680K±5%	PCS	1	R501
0200105	PORCELAIN CAPACITOR	50V 100P ±10% 5mm	PCS	6	C505,C507,C509,C511,C513,C514
0200138	PORCELAIN CAPACITOR	50V 104 ±20% 5mm	PCS	4	C504,C508,C510,C515
0200223	PORCELAIN CAPACITOR	1000V 101 +80%-20% 7.5mm	PCS	1	C503
0200228	PORCELAIN CAPACITOR	1000V 101 ±10% 7.5mm	PCS	1	C503
0200224	PORCELAIN CAPACITOR	1000V 103 +80%-20% 7.5mm	PCS	1	C502
0200267	CERAMIC CAPACITOR	CT81 250VAC221±20% 10mm	PCS	1	BC503
0200268	CERAMIC CAPACITOR	CT81 250VAC221±10% 10mm	PCS	1	BC503
0210023	TERYLENE CAPACITOR	100V 223 ±10% 5mm	PCS	1	C506
0210066	TERYLENE CAPACITOR	275V 104 ±20% 15mm	PCS	1	BC502
0210070	TERYLENE CAPACITOR	275V 104 ±10% 15mm	PCS	1	BC502
0210166	ANTI-DISTURBANCE CAPACITOR	MKP41 275VAC 103 ±20% 10	PCS	1	BC501
0260557	CD	CD11T 16V100u±20%6×12 2.5	PCS	3	TC508,TC511,TC513
0260558	CD	CD11T 25V470u±20%10×16 5	PCS	2	TC503,TC504
0260559	CD	CD11T 50V47u±20%6×12 2.5	PCS	2	TC502,TC512
0260560	CD	CD11T 10V1000u±20%8×16 3.5	PCS	4	TC505,TC506,TC509,TC510
0260527	CD	CD294 400V47U±20%22×25 10	PCS	1	TC501
0390057	MAGNETIC BEADS INDUCTOR	RH354708	PCS	1	L503
0410010	CHOKE COIL	VERTICAL 10UH 1A 5mm	PCS	1	L505
0410011	CHOKE COIL	VERTICAL 10UH 2A 5mm	PCS	2	L506,L507
0460282	SWITCHING POWER TRANSFORMER	BCK-28-0286	PCS	1	T501
0460283	SWITCHING POWER TRANSFORMER	BCK2801-624	PCS	1	T501
0570013	DIODE	HER105	PCS	4	D506,D508,D511,D512
0570028	DIODE	HER306	PCS	1	D510
0680007	SCHOTTKY DIODE	SR360	PCS	1	D509
0570014	DIODE	HER107	PCS	1	D505
0580006	VOLTAGE REGULATOR DIODE	5.1V 1/2W	PCS	1	ZD501
0580054	VOLTAGE REGULATOR DIODE	9.1V 1W	PCS	1	ZD502
0570005	DIODE	1N4007	PCS	4	D501~D504
0880765	IC	5L0380R YDTU	PCS	1	U501
0880553	IC	LM431ACZ TO-92	PCS	1	U503
0880581	IC	TL431C TO-226AA(LP)	PCS	1	U503
0880800	IC	431L TO-92	PCS	1	U503
0880888	IC	KA431AZ TO-92	PCS	1	U503
1000004	POWER GRID FILTER	UT-20 40mH ±20% 10×13	PCS	2	L501,L502
1080011	PHOTOELECTRIC COUPLER	HS817	PCS	1	U502
0880379	IC	LM7805 GOLD SEALED TO-220	PCS	1	U504
1940022	SOCKET	4P 2.0mm	PCS	1	CN501
1940030	SOCKET	10P 2.5mm	PCS	1	CN502
1940045	SOCKET	2P 8.0mm 2#	PCS	2	BCN501,BCN502
2100004	CONNECTION CORDS	Φ0.6 SHAPED 10mm	PCS	9	JP501~JP503,JP506~JP510,JP511
2100006	CONNECTION CORDS	Φ0.6 SHAPED 12.5mm	PCS	2	JP504,JP505
2300021	FUSE	T1.6AL 250V WITH PIN	PCS	1	F501
3580039	HEAT RADIATION BOARD	11×15×25 AB009K	PCS	2	U501,U504 FOR HEAT RADIATION

3580054	HEAT RADIATION BOARD	11×15×25 白 AB905	PCS	2	U501,U504 FOR HEAT RADIATION
1563276	PCB	59904S-1	PCS	1	
3870115	GROUND CHIP OF POWER BOARD	AB903	PCS	2	G501,G502
4000073	TAPPING SCREW	BT 3×8 BLACK	PCS	2	FIXED HEAT RADIATION BOARD

2. MAIN BOARD

ATERIAL CO	MATERIAL NAME	SPECIFICATIONS	UNIT	QUANTITY	LOCATION
0000009	CARBON FILM RESISTOR	1/6W100Ω±5%	PCS	1	R415
0090023	SMD RESISTOR	1/16W 10K ±5% 0603	PCS	3	R402~R404
0090192	SMD RESISTOR	1/16W 51K ±5% 0603	PCS	1	R401
0310058	SMD CAPACITOR	25V 104 +80%-20% 0603	PCS	3	C401~C403
0260206	CD	CD11C 10V100U±20%5×7 2	PCS	2	TC401,TC402
0570006	DIODE	1N4148	PCS	1	D401
1631730	PCB	49904S-1	PCS	1	
1200608	LED SCREEN	ZDC6-2102YGB-A	PCS	1	LED401
1200618	LED SCREEN	TOS-2601BG-B29	PCS	1	LED401
2360026	IR SENSOR	AT138BV3 PIN LENGTH 27mm	PCS	1	U403
1340003	LIGHT TOUCH RESTORE SWITCH	HORIZONTAL 6×6×1	PCS	3	K401~K403
0881426	IC	PT6961 SOP	PCS	1	U401
5232997	SOFT SPONGE SPACER	8×7×17.5 DOUBLE-FACED, HARD	PCS	3	2PCS FOR DISPLAY SCREEN AND MAIN BOARD, 1PC FOR IR SENSOR AND MAIN BOARD
2121516	FLAT CABLE	6-7P 100 2.0 2 SOCKET WITH L NEEDLE, THE SAME DIRECTION 6 CORD	PCS	1	XS401

3. AV BOARD

ATERIAL CO	MATERIAL NAME	SPECIFICATIONS	UNIT	QUANTITY	LOCATION
0090181	SMD RESISTOR	1/16W 100Ω ±5% 0603	PCS	1	R702
0090002	SMD RESISTOR	1/16W 2.2Ω ±5% 0603	PCS	1	R706
0310066	SMD CAPACITOR	50V 102 ±10% 0603	PCS	13	C701~C706,C716,C723~C728
0310058	SMD CAPACITOR	25V 104 +80%-20% 0603	PCS	1	C710
0310084	SMD CAPACITOR	50V 104 +80%-20% 0603	PCS	1	C710
0390095	SMD MAGNETIC BEADS	FCM1608K-221T05	PCS	8	L701~L704,L706,L708,L715,L716
0310085	SMD CAPACITOR	50V 20P ±5% NPO 0603	PCS	1	C713
0090019	SMD RESISTOR	1/16W 4.7K ±5% 0603	PCS	1	R704
0090029	SMD RESISTOR	1/16W 47K ±5% 0603	PCS	1	R715
0090017	SMD RESISTOR	1/16W 2.2K ±5% 0603	PCS	1	R710
0310234	SMD CAPACITOR	16V 105 +80%-20% 0603	PCS	2	C707,C711
0090001	SMD RESISTOR	1/16W 0Ω ±5% 0603	PCS	8	L711,L712,C717~C722
0700007	SMD DIODE	1N4148	PCS	2	D701,D702
0700001	SMD DIODE	LS4148	PCS	2	D701,D702
0700002	SMD DIODE	LL4148	PCS	2	D701,D702
0700004	SMD VOLTAGE REGULATOR DIODE	5.1V 1/2W	PCS	4	ZD701~ZD704
1563192	PCB	7969A-3	PCS	1	
0000171	CARBON FILM RESISTOR	1/4W68Ω±5%	PCS	1	R703
0000181	CARBON FILM RESISTOR	1/4W220Ω±5%	PCS	1	R701
0000286	CARBON FILM RESISTOR	1/4W2.2K±5% SHAPED 10	PCS	1	R711
0000098	CARBON FILM RESISTOR	1/6W2.2K±5% SHAPED 5	PCS	2	R712,R714
0000436	CARBON FILM RESISTOR	1/4W2K±5% SHAPED 10	PCS	1	R709
0000133	CARBON FILM RESISTOR	1/6W4.7K±5% SHAPED 7.5	PCS	1	R705
0390057	MAGNETIC BEADS INDUCTOR	RH354708	PCS	6	L705,L707,L709,L710,L713,L714
1090045	ELECTRO-OPTIC TRANSFORMER	TX179ATW	PCS	1	JK705

1090024	ELECTRO-OPTIC TRANSFORMER	TX179AT	PCS	1	JK705
1910078	TERMINAL SOCKET	AV4-8.4-6G-3	PCS	1	JK702
1910129	TERMINAL SOCKET	SA-001-012 BLACK IRON SHEET SCREEN-SHIELDED	PCS	1	JK703
1910079	TERMINAL SOCKET	AV8-8.4-6G-3	PCS	1	JK701
1940193	CABLE SOCKET	15P 1.0mm STRAIGHT DUAL LINE TOUCH POINT PLUG	PCS	1	XS701
2100010	CONNECTION CORDS	Φ0.6 SHAPED 5mm	PCS	11	JP701,JP704,JP711~JP712 ,JP721~JP727
2100003	CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	PCS	8	JP703,JP713~JP718,JP720
2100004	CONNECTION CORDS	Φ0.6 SHAPED 10mm	PCS	3	JP705,JP709,JP719
2100006	CONNECTION CORDS	Φ0.6 SHAPED 12.5mm	PCS	1	JP702
1860029	SCART SOCKET	SCART-01	PCS	1	JK706
1940026	SOCKET	3P 2.0mm	PCS	1	XS702
0200031	PORCELAIN CAPACITOR	50V 20P ±10% NPO 5mm	PCS	1	C712
0780050	TRIODE	S8050D	PCS	3	V701~V703
0000167	CARBON FILM RESISTOR	1/4W33Ω±5%	PCS	1	R708

4. OK BOARD

ATERIAL COI	MATERIAL NAME	SPECIFICATIONS	UNIT	QUANTITY	LOCATION
0000118	CARBON FILM RESISTOR	1/6W10Ω±5% SHAPED 7.5	PCS	2	R621,R622
90009	SMD RESISTOR	1/16W 330Ω ±5% 0603	PCS	1	R616
0090012	SMD RESISTOR	1/16W 560Ω ±5% 0603	PCS	1	R604
0090014	SMD RESISTOR	1/16W 1K ±5% 0603	PCS	3	R608,R611,R619
0000129	CARBON FILM RESISTOR	1/6W1K±5% SHAPED 7.5	PCS	2	R623,R625
0090023	SMD RESISTOR	1/16W 10K ±5% 0603	PCS	5	R606,R620,R618,R633,R63 4
0090026	SMD RESISTOR	1/16W 22K ±5% 0603	PCS	2	R602,R610
0090034	SMD RESISTOR	1/16W 100K ±5% 0603	PCS	2	R615,R617
0310045	SMD CAPACITOR	50V 47P ±5% NPO 0603	PCS	1	C606
0310072	SMD CAPACITOR	50V 103 ±10% 0603	PCS	1	C604
0310084	SMD CAPACITOR	50V 104 +80%-20% 0603	PCS	3	C601,C602,C608
0310058	SMD CAPACITOR	25V 104 +80%-20% 0603	PCS	3	C601,C602,C608
0260094	CD	CD110 16V47U±20%5×11 2	PCS	3	TC611,TC615,TC616
0260025	CD	CD11 16V47U±20%5×11 2	PCS	3	TC611,TC615,TC616
0260200	CD	CD11C 16V47U±20%5×7 2	PCS	3	TC611,TC615,TC616
0260127	CD	CD11 16V4.7U±20%5×11 2	PCS	2	TC602,TC604
0260021	CD	CD11 16V22U±20%5×11 2	PCS	1	TC606
0260037	CD	CD11 25V22U±20%5×11 2	PCS	1	TC606
0390095	SMD MAGNETIC BEADS	FCM1608K-221T05	PCS	1	L601
0700007	SMD DIODE	1N4148	PCS	3	VD601~VD603
0880124	IC	NJM4558D DIP	PCS	1	U601
0880308	IC	KA4558 DIP	PCS	1	U601
1980006	MICROPHONE SOCKET	CK3-6.35-106	PCS	1	MIC601
1940209	SOCKET	7P 2.0mm STRAIGHT WINDING	PCS	1	XS602
1940216	SOCKET	3P 2.0mm WINDING PLUG	PCS	1	XS601
1563436	PCB	69904S-1	PCS	1	
2100003	CONNECTION CORDS	Φ0.6 SHAPED 7.5mm	PCS	8	JP601,JP604～JP610
2100010	CONNECTION CORDS	Φ0.6 SHAPED 5mm	PCS	1	JP602
2100004	CONNECTION CORDS	Φ0.6 SHAPED 10mm	PCS	1	JP603
0000030	CARBON FILM RESISTOR	1/6W3.3K±5%	PCS	1	R628
0090224	SMD RESISTOR	1/16W 3.9K ±5% 0603	PCS	4	R627,R630~R632
0000288	CARBON FILM RESISTOR	1/4W3.9K±5% SHAPED 10	PCS	1	R629
0090106	SMD RESISTOR	1/16W 4.7Ω ±5% 0603	PCS	2	R635,R636
0260039	CD	CD11 25V47U±20%5×11 2	PCS	2	TC617,TC618
0260201	CD	CD11C 16V100U±20%6×7 2.5	PCS	3	TC619~TC621
0310207	SMD CAPACITOR	50V104 ±20% 0603	PCS	5	C612~C616
0200138	PORCELAIN CAPACITOR	50V 104 ±20% 5mm	PCS	1	C609
0881537	IC	TDA1308 SOP	PCS	1	U602
1980058	HEADPHONE SOCKET	2SJ-05231N23	PCS	1	JK603
1980060	HEADPHONE SOCKET	2SJ-05232N23	PCS	1	JK603
0090030	SMD RESISTOR	1/16W 56K ±5% 0603	PCS	2	R624,R626

4. DECODE BOARD

ATERIAL CO	MATERIAL NAME	SPECIFICATIONS	UNIT	QUANTITY	LOCATION
0090001	SMD RESISTOR	1/16W 0Ω ±5% 0603	PCS	37	C2119,C2128,C2131,L210~L215,R201~R204,R212,R226,R228,R234,R236,R245,R247,R222,R251,R255,R257,R258,R282,R298,R299,R303,R318,R331,R2159,R297,R2205,R2110,R279,R268
0090006	SMD RESISTOR	1/16W 75Ω ±5% 0603	PCS	7	R233,R261,R270,R273,R274,R276,R280
0000375	CARBON FILM RESISTOR	1/4W2.2Ω±5%	PCS	1	R326
0090272	SMD RESISTOR	1/16W1Ω±5% 0603	PCS	6	R304~R307,R321,R340
0090003	SMD RESISTOR	1/16W 10Ω ±5% 0603	PCS	2	R301,R302
0090005	SMD RESISTOR	1/16W 33Ω ±5% 0603	PCS	16	R251,R252,R256,R265~R267,R291~R296,R2162
0090232	SMD RESISTOR	1/16W 150Ω ±5% 0603	PCS	1	R2180
0090008	SMD RESISTOR	1/16W 220Ω ±5% 0603	PCS	4	R2168~R2171
0090009	SMD RESISTOR	1/16W 330Ω ±5% 0603	PCS	1	R2105
0090011	SMD RESISTOR	1/16W 470Ω ±5% 0603	PCS	2	R325,R327
0090013	SMD RESISTOR	1/16W 680Ω ±5% 0603	PCS	2	R259,R260
0090014	SMD RESISTOR	1/16W 1K ±5% 0603	PCS	27	L225,R213,R215,R2101,R2102,R2104,R2117,R2118~R2128,R254,R2184,R2160,R2161,R2191,R350,R352,R286,R2109
0090223	SMD RESISTOR	1/16W 2K ±5% 0603	PCS	1	R2103
0090016	SMD RESISTOR	1/16W 1.5K ±5% 0603	PCS	3	R323,R324,R243
0090249	SMD RESISTOR	1/16W 510Ω ±5% 0603	PCS	1	R214
0090018	SMD RESISTOR	1/16W 3.3K ±5% 0603	PCS	1	R242
90019	SMD RESISTOR	1/16W 4.7K ±5% 0603	PCS	21	R238~R240,R2130,R2131,R2134,R2135,R2138~R2140,R2142,R2143,R2146,R2147,R2150,R2151,R2182,R2183,R2189,R2190,R2206
0090021	SMD RESISTOR	1/16W 6.8K ±5% 0603	PCS	8	R2136,R2148,R2152~R2155,R376,R2100
0090023	SMD RESISTOR	1/16W 10K ±5% 0603	PCS	22	1,R313,R314,R329,R330,R339,R2164,R2200,R2201,R2167,R2198,R2199,R351,R353,R290,R2202,R2106,R2108
0090024	SMD RESISTOR	1/16W 15K ±5% 0603	PCS	2	R209,R223
0090025	SMD RESISTOR	1/16W 20K ±5% 0603	PCS	4	R211,R312,R315,R316
0090255	SMD RESISTOR	1/16W24K±5% 0603	PCS	8	R2129,R2133,R2137,R2141,R2145,R2149,R2181,R2188
0090188	SMD RESISTOR	1/16W 18K ±5% 0603	PCS	1	R210
0090029	SMD RESISTOR	1/16W 47K ±5% 0603	PCS	1	R289
90197	SMD RESISTOR	1/16W 150K ±5% 0603	PCS	2	R319,R320
0090231	PRECISION SMD RESISTOR	1/16W 680K ±1% 0603	PCS	2	R317,R322
0090319	PRECISION SMD RESISTOR	1/16W 750K ±1% 0603	PCS	1	R227
0090034	SMD RESISTOR	1/16W 100K ±5% 0603	PCS	16	R224,R308,R310,R2111~R2116,R246,R2186,R2193,R364,R366,R373,R375
0260019	CD	CD11 16V10U±20%5×11 2	PCS	29	TC201,TC202,TC217,TC221~TC233,TC236,TC240,TC241,TC323,TC322,TC347,TC320,TC321,TC348,TC249,TC203,TC318,TC244
0260126	CD	CD11 16V1U±20%5×11 2	PCS	2	TC242,TC243
0260028	CD	CD11 16V220U±20%6×12 2.5	PCS	10	TC207~TC209,TC211,TC213,TC235,TC345,TC301,TC342,TC245

0260025	CD	CD11 16V47U±20%5×11 2	PCS	13	TC204~TC206,TC210,TC234,TC237,TC302~TC304,TC308,TC309 ,TC247,TC248
0310085	SMD CAPACITOR	50V 20P ±5% NPO 0603	PCS	1	C222
0310190	SMD CAPACITOR	50V 27P ±5% NPO 0603	PCS	2	C275,C276
0310045	SMD CAPACITOR	50V 47P ±5% NPO 0603	PCS	17	C266,C289,C290,C292,C293,C295,C296,C298,C299,C2101,C2102,C2104,C2105,C262~C265
0310047	SMD CAPACITOR	50V 101 ±5% NPO 0603	PCS	10	C233,C2111,C2114,C2117,C2120,C2123,C2126,C206,C2159,C2183
0310051	SMD CAPACITOR	50V 331 ±5% NPO 0603	PCS	2	C212,C213
0310048	SMD CAPACITOR	50V 151 ±5% NPO 0603	PCS	2	C304,C306
0310084	SMD CAPACITOR	50V 104 +80%-20% 0603	PCS	84	C207,C211,C214,C216,C217,C224,C226~C231,C234~C239,C241~C254,C256~C259,C267~C274,C279,C301~C303,C305,C309,C311,C312,C2138~C2140,C2153~C2157,C2161,C2163,C2169,C2166,C2174,C2175,C2168,C2100,C2179,C2181,C2180,C356,C357,C2164,C2171,C2167,C2176,C2177,C2178,C2150~C2152,C287,C284
0310058	SMD CAPACITOR	25V 104 +80%-20% 0603	PCS	84	C207,C211,C214,C216,C217,C224,C226~C231,C234~C239,C241~C254,C256~C259,C267~C274,C279,C301~C303,C305,C309,C311,C312,C2138~C2140,C2153~C2157,C2161,C2163,C2169,C2166,C2174,C2175,C2168,C2100,C2179,C2181,C2180,C356,C357,C2164,C2171,C2167,C2176,C2177,C2178,C2150~C2152,C287,C284
0310234	SMD CAPACITOR	16V 105 +80%-20% 0603	PCS	8	C201~C204,C221,C240,C285,C286
0310066	SMD CAPACITOR	50V 102 ±10% 0603	PCS	11	C2112,C2115,C2118,C2121,C2124,C2127,C223,C278,C2146,C2148,C288
0310231	SMD CAPACITOR	50V 122 ±10% 0603	PCS	8	C2122,C2129,C2130,C2133,C2135,C2136,C2145,C2147
0310067	SMD CAPACITOR	50V 152 ±10% 0603	PCS	1	C215
0310068	SMD CAPACITOR	50V 222 ±10% 0603	PCS	2	C307,C310
0310201	SMD CAPACITOR	50V 153 ±10% 0603	PCS	1	C210
0310202	SMD CAPACITOR	50V 223 ±10% 0603	PCS	1	C2184
0310055	SMD CAPACITOR	16V 333 ±10% 0603	PCS	1	C225
0310056	SMD CAPACITOR	16V 473 ±10% 0603	PCS	2	C219,C220
0310362	SMD CAPACITOR	16V474 +80%-20% 0603	PCS	1	C218
0390044	SMD INDUCTOR	10UH ±10% 2012	PCS	2	L303,L306
0390096	SMD INDUCTOR	1.8UH ±10% 1608	PCS	6	L243~L248
0390057	MAGNETIC BEADS INDUCTOR	RH354708	PCS	11	L205,L209,L217,L220,L221,L222,L223,L227,L228,L226.L302

0390095	SMD MAGNETIC BEADS	FCM1608K-221T05	PCS	39	L201,L203,L207,L208,L224,L234~L236,L238,L250,L309,L229~L233,L301,L304,L305,L307,L308,L310~L312,L314,L316~L324,L325,L326,L327,L218,L219
0390087	SMD MAGNETIC BEADS	FCM2012V-221T07	PCS	2	L254,L255
0090106	SMD RESISTOR	1/16W 4.7Ω ±5% 0603	PCS	1	L206
0700007	SMD DIODE	1N4148	PCS	18	VD201,VD205~VD221
0700001	SMD DIODE	LS4148	PCS	18	VD201,VD205~VD221
0700002	SMD DIODE	LL4148	PCS	18	VD201,VD205~VD221
0780085	SMD TRIODE	8050D	PCS	3	Q301,Q302,Q203
0780029	TRIODE	C8050	PCS	2	V307,V308
0780030	TRIODE	8550C	PCS	3	V306,V309,Q303
0780062	SMD TRIODE	9014C	PCS	1	V310
0780033	TRIODE	9015C	PCS	1	Q204
0780020	TRIODE	C1815Y	PCS	1	Q212
0780197	SMD TRIODE	C1815	PCS	8	Q205~Q210,Q223,Q224
0780043	TRIODE	2SA1015	PCS	3	Q211,Q218,Q219
0780040	SMD TRIODE	3904	PCS	1	V305
0780193	SMD TRIODE	2SK3018	PCS	2	V303,V304
0780115	SMD TRIODE	2SB1132	PCS	2	V301,V302
0880185	IC	NJM4558M SOP	PCS	4	U219，U220，U221,U215
0880562	IC	4580 SOP	PCS	4	U219，U220，U221,U215
0880361	IC	4558 SOP	PCS	4	U219，U220，U221,U215
0880322	IC	MM74HCU04M SOP	PCS	1	U205
0880513	IC	HCU04 SOP	PCS	1	U205
0881415	IC	HY57V641620HGT-7 TSOP	PCS	1	U211
0881872	IC	KSV464P4JA-70 TSOP	PCS	1	U211
0881182	IC	LM1117MP-ADJ SOT-223	PCS	1	U209
0881057	IC	CS4360 SSOP	PCS	1	U207
0881059	IC	CS5333 SSOP	PCS	1	U210
0881031	IC	24C02N SOP	PCS	1	U202
0881897	IC	MT1389EE QFP	PCS	1	U201
0881994	IC	MT1389FE QFP	PCS	1	U201
0881378	IC	BA5954FP HSOP	PCS	1	U302
0881886	IC	36C7T 3MCD4052BM SOP	PCS	1	U304
0960020	CRYSTAL OSCILLATOR	27.00MHz 49-S	PCS	1	X201
1940072	CABLE SOCKET	6/5P 1.25mm STRAIGHT DUAL LINE PLUG	PCS	1	XS205
1940193	CABLE SOCKET	15P 1.0mm STRAIGTH DUAL LINE TOUCH POINT PLUG	PCS	1	XS204
1631529	PCB	2967S-2	PCS	1	
1940024	SOCKET	5P 2.0mm	PCS	1	XS302
1940023	SOCKET	7P 2.0mm	PCS	1	XS201
1940005	SOCKET	6P 2.0mm	PCS	1	XS303
1940171	SOCKET	13P 2.5mm	PCS	1	XS203
1940094	CABLE SOCKET	24P 0.5mm SMD WITH CLASP	PCS	1	XS301

11. APPENDIX-AM/FM Tuner Specificadtion

AM/FM Tuner Specification

イホソシ

			TFCF1U800A
END CUST	CUST	CUST MODEL NO.	ALPS MODEL NO.

					APPD	CHKD	DSGD	
								TITLE PRODUCT **TFCF1U** SPECIFICATION
					DOCUMENT NO.			
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				0/11

AM/FM Tuner Specification

1.Application product P/N TFCF1U TYPE FM/AM TUNER

1-1.Manufacturing location Japan and People Republic of China and Malaysia

2.Specification Customer Specification USA / CND Version

3.Test conditions

Usual standard test with next condition

Measurement shall be started to minutes after power applied

The apply voltege must be regulated +9 v ± 2%

Condition Temperature :5。ｵ35。

Humidity :45。ｵ85 % Rh

If there is an objection to test result, they set up with next test condition

Condition Temperature :20±2。

Humidity :60。ｵ70 % Rh

Unit: Scale / Tolerance

	Components	Materials Finish/ Specifications				Components	Materials Finish/ Specifications		
1			6						
2			7						
3			8						
4			9						
5			1		0				

					DSGD.			
					CHKD.	TITLE PRODUCT		
						TFCF1U SPECIFICATION		
					APPD			
						(1/11)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4.General Specifications

4-1.FM Tuner General Specifications

Frequency Range	87.5MHz。ォ108.0MHz
STEP Frequency	50KHz/100KHz
Intermediate Frequency	10.7MHz(Upper Heterodyne)
Operating Temperature	ィC20。ォ」ォ70。
ANT Input Impedance	75 Unbalanced

4-2. PLL General Specifications

Cutout port function		B01	B02					
		FM/AM	。ェ					
Seral date	0	AM	。ェ					
	1	FM	。ェ					

Crystal Frequency :75KHz

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(2/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

4-3.AM Tuner General Specifications

Frequency Range	530KHz｡ｵ1710KHz
STEP Frequency	10KHz or 9KHz
Intermediate Frequency	450KHzｺﾕ(Upper Heterodyne)
Operating Temperature	ｲC20｡ｵﾚｵ70｡
ANT Input Impedance	Use Dummy antenna which specified If there hanppened,should use loop antenna

5.Machanical specifications

Dimensions	See Assembly drawing
Core torque	3｡ｵ30mN·m
Variable Resistor Torque	3｡ｵ30mN·m
Antenna Connector	FMﾚﾕSticker S DIN 45325/F AMﾚﾕSMK LPR0210-XX09 or ﾏ犒高ｱﾆｷ

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(3/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-1.Terminal load connections」ユ

Specified jig should be used for measurement

Jig circuit follows 10-2

During FM measurement,use specified by IHF T-200(200Hz。ォ15KHz B.P.F)

Filter for audio output of filer *Less than 200Hz 」ユ18dB/act.out

*220Hz and 15KHz」ユ-3dB MIN

19KHz」ユ-30dB MAX

6-2.Standard connection diagram

FM section」ユ

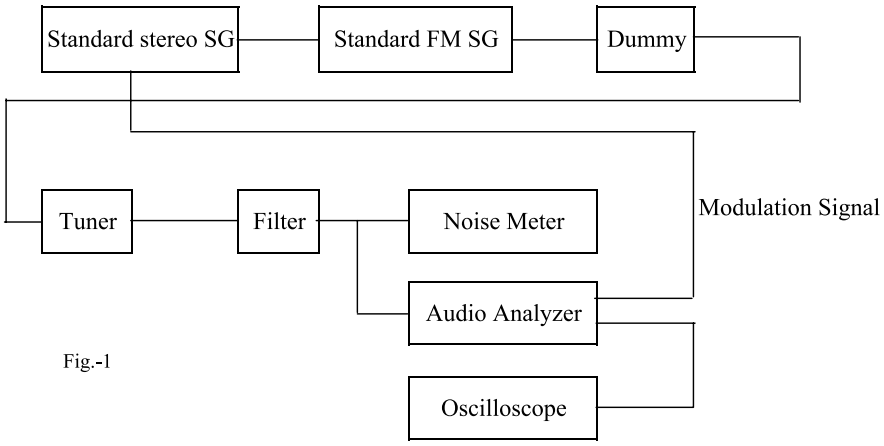


Fig.-1

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(4/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

6-3.Test Modulation

FM」ｺMONO 1KHz 75.0KHz dev

STEREO 1KHz L」ｵR 67.5KHz dev

PILOT 7.5KHz dev

Antenna Input 75ﾗｸ Opened SSG-Dunmy los

RF Input Level 60dBu

AM」ｺ400hz 30% mod

Use Dunmy antenna which specified by ALPS.

RF Input level」ｺ94dBu(ANT Input)

7.DC Specification

ITEM	TEST Condition	SPEO ｹ貂			UNIT
		MIN	TYP	MAX	ｵ･ﾎｻ
Supply Voltage 」ｵ9v	Off Station	8.5	9	9.5	V
Supply Currant 」ｵ9v	Off Station	。I	65	90	mA

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(5/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

8.FM Tuner Electrical Specification (Measurement Points Unless Otherwise Stated are 87.5,98,100MHz.
Concerning MONORAL test shall be at L out terminal)

ITEM	TEST Condition			SPEC ヶ貂			UNITヶ貂
				MIN	TYP	MAX	
50dB S/N Sensitivity			87.5MHz	。I	17	25	dBu
			98.0MHz	—	15	25	
			106.0MHz	。I	17	25	
IHF Sensitivity	Distortion 3%		87.5MHz	。I	14	20	dBu
			98.0MHz	。I	12	20	
			106.0MHz	。I	14	20	
Max S/N Ratio		MONO	98.0MHz	65	72	。I	dB
		STEREO	98.0MHz	60	67	。I	
Distortion		MONO	98.0MHz	。I	0.2	1.5	%
		STEREO	98.0MHz	。I	0.3	2	
Distortion with strong signal	120dBu	MONO	98.0MHz	。I	0.2	2	%
		STEREO	98.0MHz	。I	0.3	2.5	
Audio Output Level	L and R out	MONO	98.0MHz	0	3	6	dBs
		STEREO	98.0MHz	-1	2	5	
Stereo Separation			98.0MHz	25	40	—	dB
Stereo Work Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Tuned Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	18	27	dBu
Auto Stop Level	SDCOJ⊐0 SDCTJ⊐0		98.0MHz	10	20	33	dBu

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
								(6/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

ITEM	TEST Condition		SPEC ケ貂			UNITケ貂
			MIN	TYP	MAX	
Image Rejection	MONO	98.0MHz	17	23	—	dB
Carrier Leak		98.0MHz	28	33	—	dB
Emphasis	-12.29 IHF Filter Off	98.0MHz	-3	0	3	dB
Pilot Margin		98.0MHz	4	10	—	dB
Adjacent Channel Selectivity	±400KHz	98.0MHz	20	30	—	dB
AM Rejection		98.0MHz	40	60	—	dB
I.F. Rejection		98.0MHz	60	90	—	dB
Spurious Response Patio		98.0MHz	40	50	—	dB
Spurious Radiation	Meat FOC Requirements Note1.		3	10	—	dB
Antenna Leakage	Meat FOC Requirements Note1.		3	8	—	dB

Note1.Spurlous Radiation and Antenna Leakage 」ヨUse Radio Set Provided by CUSTMOR

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(7/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

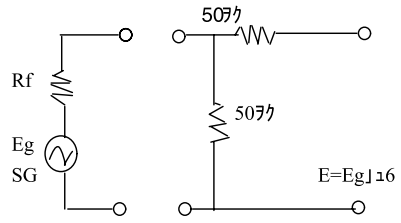
9.AM Tuner Electrcical Specification (Test shall be at L out Terminal)

ITEM	TEST Condition		SPEC ㄅ貂			UNITㄅ貂
			MIN	TYP	MAX	
S/N 20dB Sensitivity		620KHz	—	54	61	dBu
		1050KHz	—	48	57	
		1490KHz	—	48	56	
Max S/N		1050KHz	43	54	—	dB
Distortion		1050KHz	—	1.3	2.5	%
Distortion with Strong Signal	104dBu RF Input Level	1050KHz	—	1.3	2.5	%
Audio Output Level	L.R OUT	1050KHz	-11	-7	—	dBs
One Signal Selectivity	±10KHz	1050KHz	18	27	—	dB
Image Rejection		1050KHz	30	36	—	dB
I.F. Rejection		1050KHz	45	55	—	dB
AGC Form		1050KHz	44	50	—	dB
Audio Frequency Response	O Point 400Hz 100Hz	1050KHz	-10	-5.5	—	dB
	Refㄱ400Hz 4KHz	1050KHz	-22	-16	—	
Auto stop level		1050KHz	—	50	66	dBu
Tuned Level		1050KHz	—	52	61	dBu

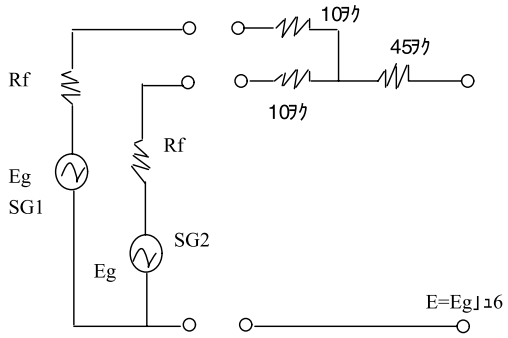
					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			
							(8/11)	
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

10-1.ANT PAD

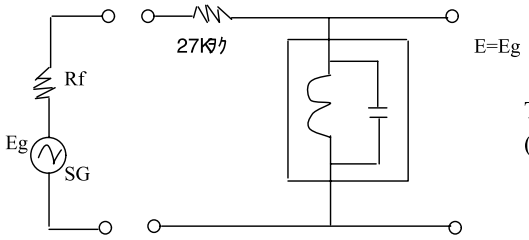
(1).FM1 SIGNAL



(2).FM2 SIGNAL



(3).AM1 SIGNAL



Trans mand TOKO
(LイP15.2uH , C=30PF)

ANT Input Signal Voltage is Open Voltage ON SSG

NOTE」ユUse Test jig which specified

Rf = 50ヲク

					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(9/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

11.Printed-Wiring Board Material

ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL － 437F	MCL － 437F	MCL － 437F
UL Grade	94V － 0	94V － 0	94V － 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S△	NE M PF2△	PNE － 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

Material Suppliar	SUZHOU Matsushita Electric Work Co.,LTD	Suzhou Matsushita Electric Work Co.,LTD
Trade Name	R8700	R8700
UL Grade	94V － 0	94V － 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP－N870A－T YMEW－N870A－T	SMEW－N870A－T
UL File NO.	E107496 (S)	E164387 (S)

Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE		PRODUCT
						TFCF1U		SPECIFICATION
					APPD			
								(11/E)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

Description of DI control Data

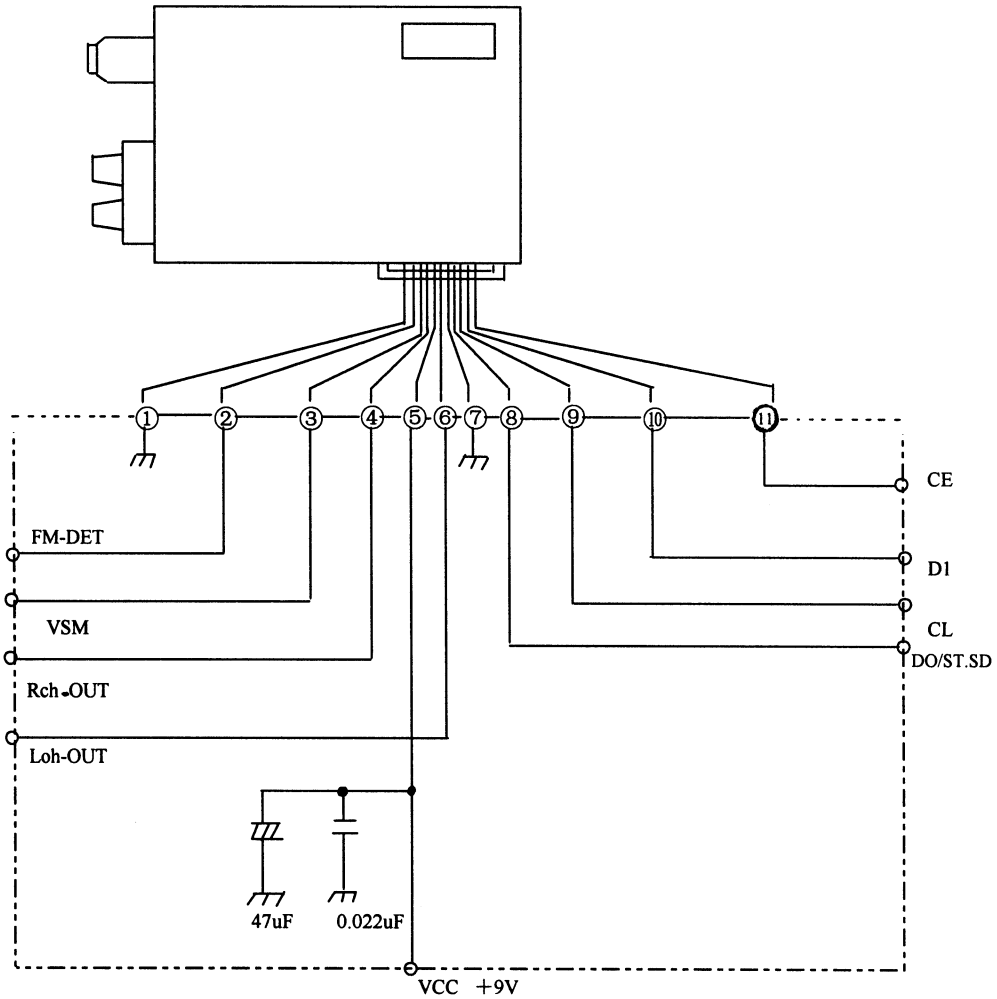
<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
<tr><td>1</td><td>*</td><td>P0</td><td>272 to 65535</td><td>Twice the set value</td></tr>
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

10-2. TEST JIG

NOTE: Use Test jig which specified



					DSGD.			
					CHKD.	TITLE	PRODUCT	
						TFCF1U	SPECIFICATION	
					APPD			(10/11)
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

11.Printed-Wiring Board Material

ITEM	Contants		
Material Suppliar	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD	Hitachi Chemical CO.,LTD
Trade Name	MCL ｣ｪ 437F	MCL ｣ｪ 437F	MCL ｣ｪ 437F
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0	94V ｣ｪ 0
Edging Supplier	NIPPON ELEC Co.,LTD	NIPPON ELEC Co.,LTD	PNE PCB LTD.
UL Type Designation	NE 49S。	NE M PF2。	PNE ｣ｪ 1B
UL File NO.	E41166 (S)	E41166 (S)	E67640

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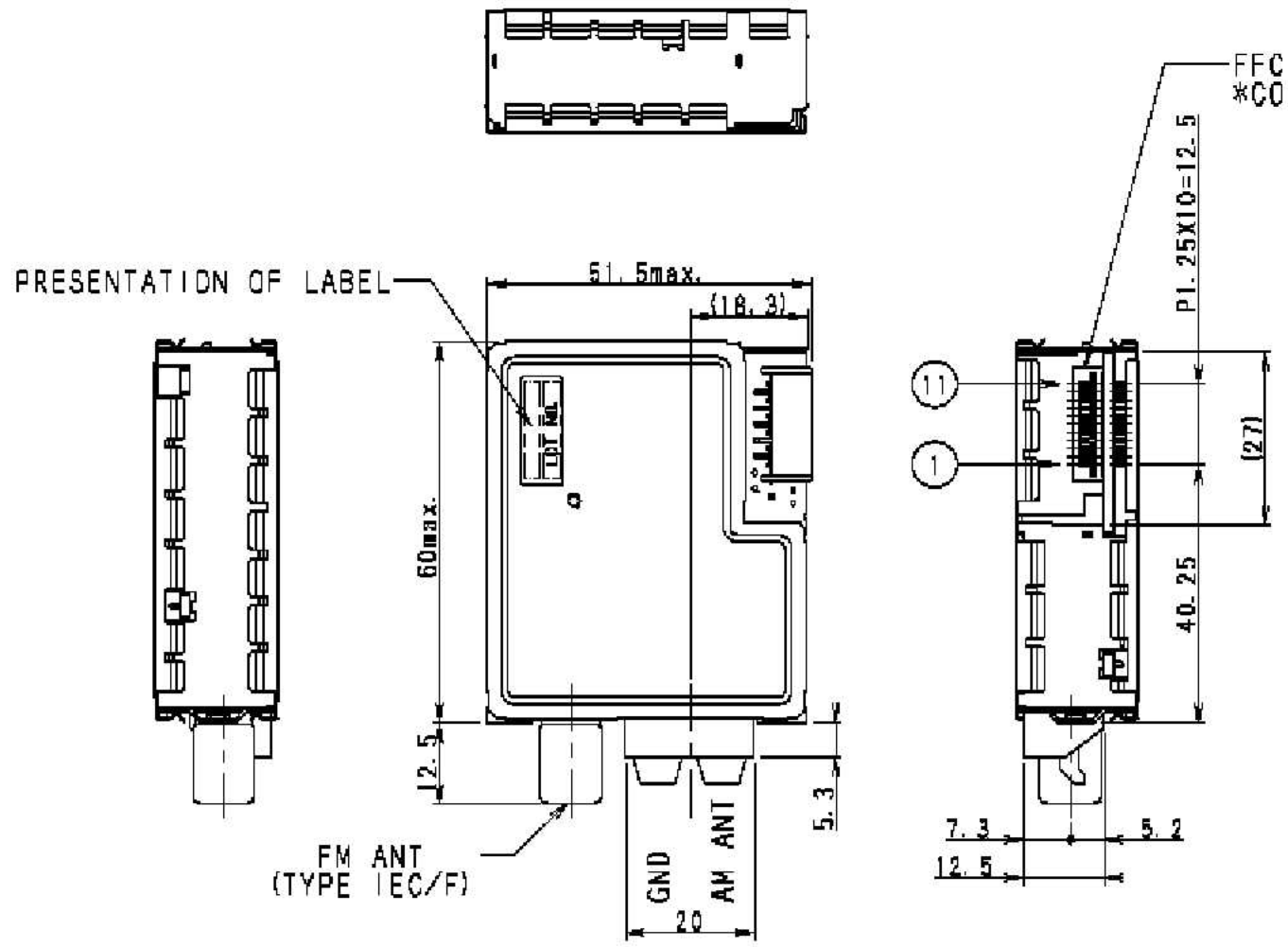
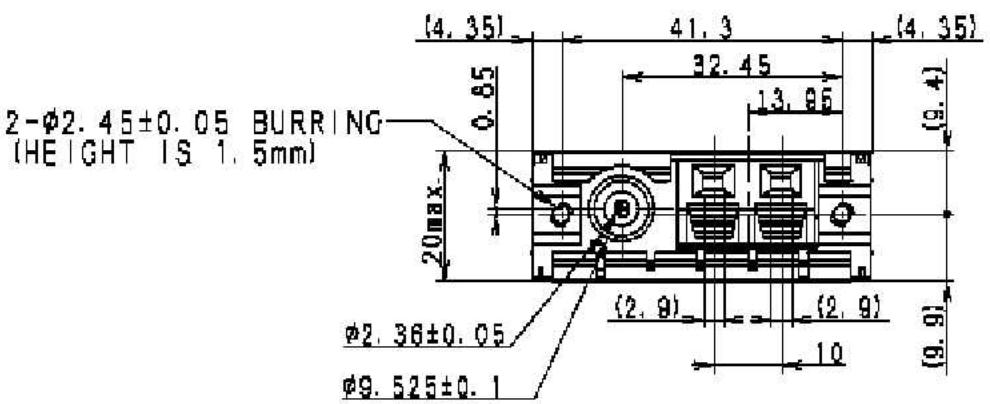
Trade Name	R8700	R8700
UL Grade	94V ｣ｪ 0	94V ｣ｪ 0
Etching Supplier	Yamanashi Matsushita Elactic Work Co.,LTD	Suzhou Matsushita Electric Works(PWB) Co.,LTD
UL Type Designation	NTP｣ｪN870A｣ｪT YMEW｣ｪN870A｣ｪT	SMEW｣ｪN870A｣ｪT
UL File NO.	E107496 (S)	E164387 (S)

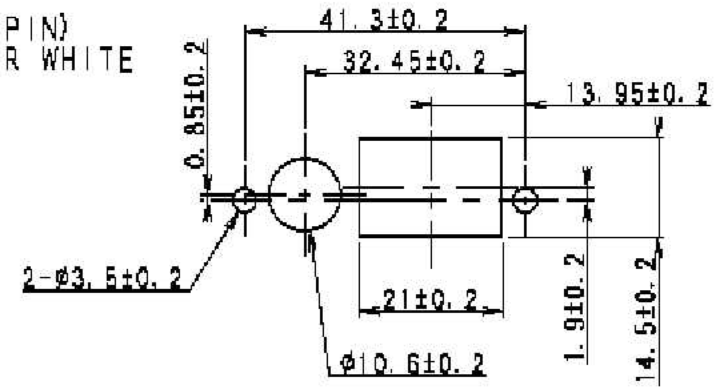
Dimension of Print-Wiring Board	56 × 49

					DSGD.			
					CHKD.	TITLE PRODUCT **TFCF1U** SPECIFICATION		
					APPD	(11/E)		
SYNB.	DATE CR NO.	APPD	CHKD.	DSGD.				

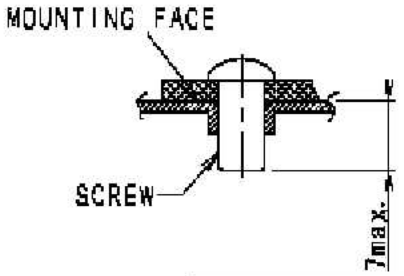




RECOMMENDED MOUNTING HOLE(REFERENCE ONLY)



NOTE 1. TOLERANCES ARE ±0.5mm.
UNLESS OTHERWISE SPECIFIED.
2. ALPS CAN ALTER COVER HOLE DESIGN
WITHOUT NOTICE IF NO ELECTRICAL DEGRADATION.
3. SCREW LENGTH FROM MOUNTING FACE IS 8mm MAX.



No.	NAME
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

		TFCF1U
PRESENTATION OF LABEL	CUST PARTS NO.	ALPS MODEL NO.

PART NO.	NAME	MATERIAL	SPEC.	FINISH

ZONE	SYMB.	DATE OR NO.	APPD.	CHKD.	DSGD.
C-5	B1	Sep. 9.'02	M. K	Y. S	J. K
D-1	A1	K020108	H. O	Y. S	J. K

DSGD. CHKD. APPD.

SCALE 1:1

UNIT mm

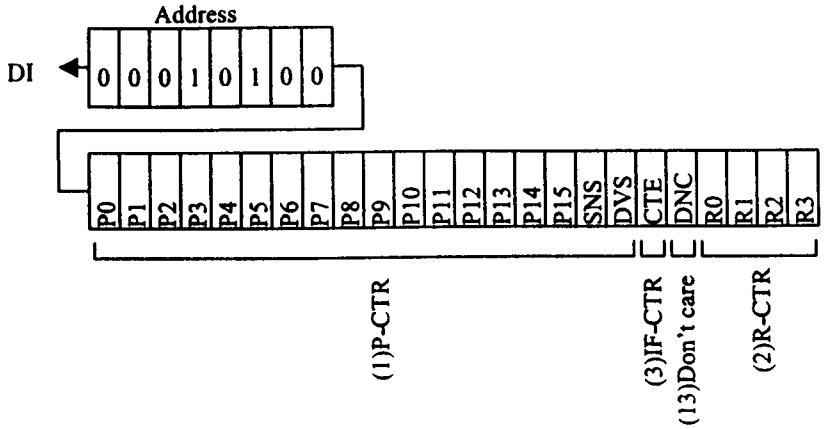
TITLE TFCF1 ASSEMBLY DRAWING

KEY NO. U111A6 (A3・■■用紙)

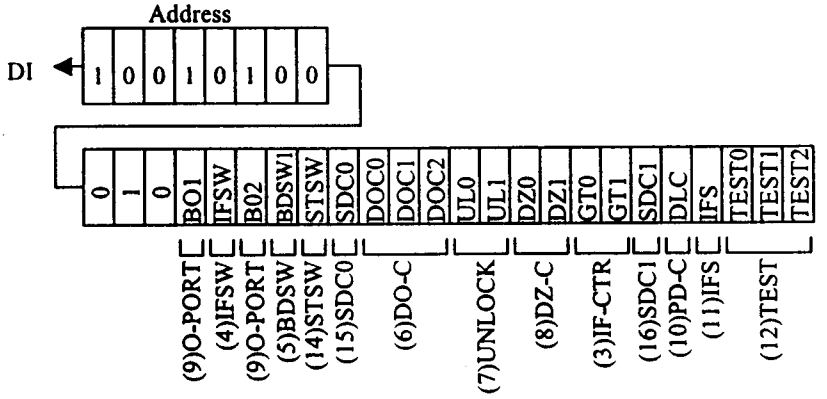
59

Composition of DI control data (serial data input)

(1) IN mode



(2) IN2 mode



Description of DI control Data

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<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(1)</td><td>Programmable divider data

P0 to P15
DVS,SNS</td><td>
• Data to set the dividing number of programmable divider
Binary value with P15 assued to be MSB. LSB varies according to DVS and SNS.
(*: don't care)
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<tr><th>DVS</th><th>SNS</th><th>LSB</th><th>set dividing number(N)</th><th>actual dividing number</th></tr>
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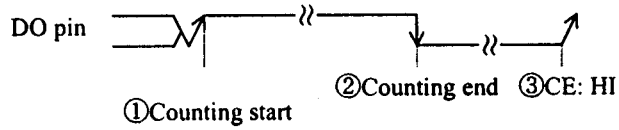
<tr><td>0</td><td>1</td><td>P0</td><td>272 to 65535</td><td>Set value</td></tr>
<tr><td>0</td><td>0</td><td>P4</td><td>4 to 4095</td><td>Set value</td></tr>
</table>
* P0 to P3 invalid when LSB:P4
• To select the signal input (FMIN, AMIN) to the programmable divider and to change the input frequency range.
(*: don't care)
<table>
<tr><th>DVS</th><th>SNS</th><th>Input</th><th>Operation frequency range</th></tr>
<tr><td>1</td><td>*</td><td>FMIN</td><td>10 to 160MHz</td></tr>
<tr><td>0</td><td>1</td><td>AMIN</td><td>2 to 40MHz</td></tr>
<tr><td>0</td><td>0</td><td>AMIN</td><td>0.5 to 10MHz</td></tr>
</table>
</td><td></td></tr>
<tr><td>(2)</td><td>Reference divider data

R0 to R3</td><td>
• Reference frequency (fref) selection data
<table>
<tr><th>R3</th><th>R2</th><th>R1</th><th>R0</th><th>Reference frequency</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>25</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>6.25</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>3.125</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>3.125</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>15</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>PLL INHIBIT + X'tal OSC STOP</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>PLL INHIBIT</td></tr>
</table>
* PLL INHIBIT
• The programmable divider and IF counter stop, with FMIN,AMIN, and IFIN inputs being in the pull-down condition (GND), and the charge pump has the high impedance.
</td><td></td></tr>
</table>

<table>
<tr><td>(3)</td><td>CTE
GT0,GT1</td><td>
<table>
<tr><th>GT1</th><th>GT0</th><th>Counting time</th><th>Wait time</th></tr>
<tr><td>0</td><td>0</td><td>4 ms</td><td>3 to 4 ms</td></tr>
<tr><td>0</td><td>1</td><td>8</td><td>3 to 4</td></tr>
<tr><td>1</td><td>0</td><td>16</td><td>3 to 4</td></tr>
<tr><td>1</td><td>1</td><td>32</td><td>3 to 4</td></tr>
</table>
</td><td>IFS</td></tr>
<tr><td>(4)</td><td>MUTE control data
IFSW</td><td>• Data to determine the output of output port IFSW, controlling the MUTE function.
"Data"=0: at receiving
1: MUTE</td><td></td></tr>
<tr><td>(5)</td><td>FM/AM BAND selection control data
BDSW</td><td>• Data to determine the output of output port BDSW, controlling selection of BAND.
"Data"=0: AM
1: FM</td><td></td></tr>
<tr><td>(6)</td><td>DO pin control data

DOC0
DOC1
DOC2</td><td>• Data to control DO pin output
<table>
<tr><th>DOC2</th><th>DOC1</th><th>DOC0</th><th>DO pin condition</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Low when unlock is detected.</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>end-UC(See the item with asterisk below)</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Open</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Low when SDON</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Low when stereo</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Open</td></tr>
</table>
• The open condition is selected at power ON/reset.
* IF counter counting end check
 

① With end-UC set and IF counter starting (CTE=0→1), DO pin opens automatically.
② At end of counting of the IF counter, DO pin goes LOW and check on counting end can be made.
③ DO pin opens when serial data is entered/output (CE pin: Hi)
Note: DO pin is always in the open condition during data input (IN1 and IN2 modes, during CE: Hi period), regardless of DO pin control data (DOC0 to 2). In the DO pin condition during data output (OUT mode, CE-Hi period), the content of internal DO serial data is output in synchronization with CL, regardless of DO pin control data (DOC).</td><td>UL0,UL1
CTE</td></tr>
</table>

<table>
<tr><th>No.</th><th>Control block data</th><th>Description</th><th>Related data</th></tr>
<tr><td>(7)</td><td>Unlock detection data

UL0,UL1</td><td>• Phase error (ϕE) detection width selection data to judge if PLL is locked.
Phase error exceeding the detection width is judged that PLL is locked
(*:don't care)
<table><tr><th>UL1</th><th>UL0</th><th>ΦE Detection width</th><th>Detection output</th></tr><tr><td>0</td><td>0</td><td>Stop</td><td>Open</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Direct output of ϕE</td></tr><tr><td>1</td><td>*</td><td>±6.67μ</td><td>ϕE extended by 1 to 2 ms</td></tr></table>* DO pin is LOW. Serial data output: UL = 0.</td><td>DOC0
DOC1
DOC2</td></tr>
<tr><td>(8)</td><td>Phase comparator control data

DZ0,DZ1</td><td>• Data to control the dead zone of phase comparator
<table><tr><th>DZ1</th><th>DZ0</th><th>Dead zone mode</th></tr><tr><td>0</td><td>0</td><td>DZA</td></tr><tr><td>0</td><td>1</td><td>DZB</td></tr><tr><td>1</td><td>0</td><td>DZC</td></tr><tr><td>1</td><td>1</td><td>DZD</td></tr></table>Dead zone width: DZA<DZB<DZC<DZD</td><td></td></tr>
<tr><td>(9)</td><td>Output port data

$\overline{BO1}$,$\overline{BO2}$</td><td>• Data to determine the output of output ports $\overline{BO1}$ and $\overline{BO2}$
"Data"=0: OPEN
1: Low</td><td></td></tr>
<tr><td>(10)</td><td>Charge pump control data

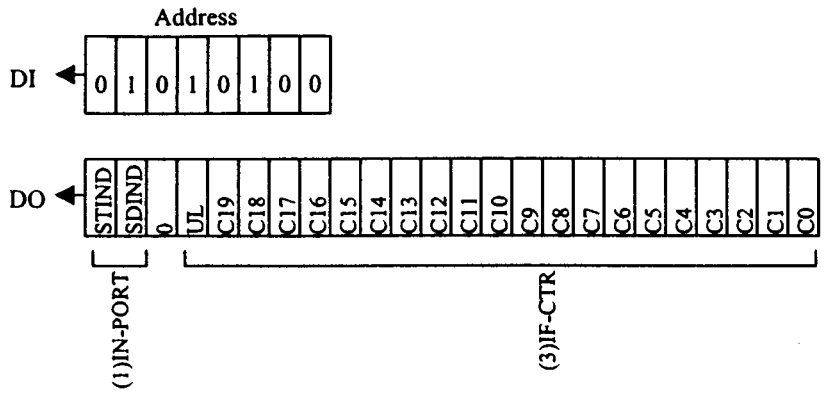
DLC</td><td>• Data to enforce control of charge pump output
<table><tr><th>DLC</th><th>Charge pump output</th></tr><tr><td>0</td><td>Normal</td></tr><tr><td>1</td><td>Forced to LOW</td></tr></table>In case of dead lock because of VCO oscillation stop when the VCO control voltage (Vtune) is 0 V, it is possible to clear dead lock by setting the charge pump output to LOW and V tune to Vcc. (Dead lock clear circuit)</td><td></td></tr>
<tr><td>(11)</td><td>IFS</td><td>• Normally, set Data = 1. Setting Data = 0 causes the input sensitivity worsening mode and the sensitivity decreases by about 10 to 30mVrms.</td><td></td></tr>
<tr><td>(12)</td><td>LSI test data
TEST0 to 2</td><td>• LSI test data
TEST0
TEST1] All to be set to "0"
TEST2
All set to zero at power ON/reset</td><td></td></tr>
<tr><td>(13)</td><td>DNC</td><td>• Set data = 0.</td><td></td></tr>
<tr><td>(14)</td><td>Forced monaural control data

STSW</td><td>• Data to determine the output of output port STSW, controlling the forced stereo functions.
"Data"=0: MONO
1: STEREO</td><td></td></tr>
<tr><td>(15)
(16)</td><td>SD sensitivity control data

SDC0
SDC1</td><td>• Data to determine the output of output ports SDC0 and SDC1, controlling the SD sensitivity
"Data"=SDC0: 0, SDC1: 0 → SD sensitivity = 42dBuV (Typ)
SDC0: 0, SDC1: 1 → SD sensitivity = 45dBuV (Typ)
SDC0: 1, SDC1: 0 → SD sensitivity = 51dBuV (Typ)
SDC0: 1, SDC1: 1 → SD sensitivity = 56dBuV (Typ)</td><td></td></tr>
</table>

DO control data (serial data output) composition

(1) OUT mode

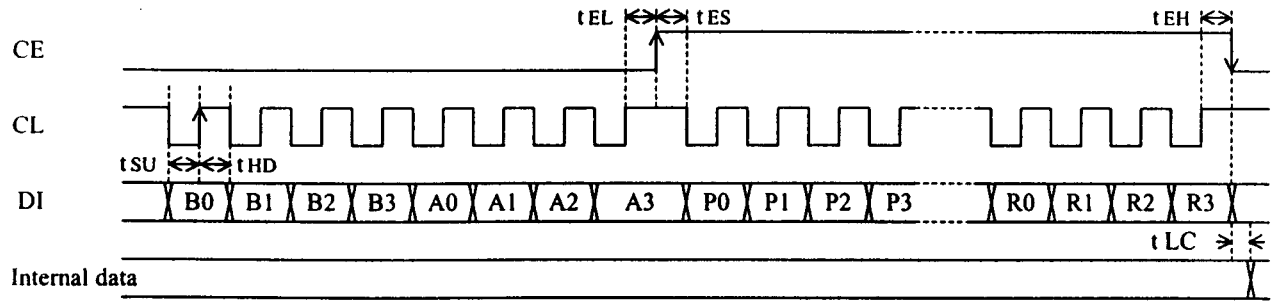


Description of the DO output data

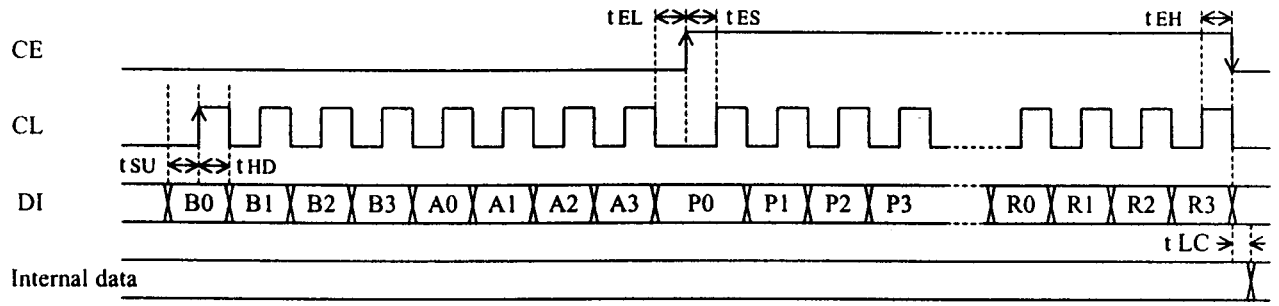
No.	Control block data	Description	Related data
(1)	Stereo and SD indicators control data STIND, SDIND	• Data latching stereo and SD indicator conditions. Latching made in the data output (OUT) mode. STIND ← Stereo indicator condition 0: ST ON, 1: ST OFF SDIND ← SD indicator condition 0: SD ON, 1: SD OFF	
(2)	PLL unlock data UL	• Data latching the content of unlock detection circuit UL ← 0: At unlock 1: At lock or detection stop mode	UL0 UL1
(3)	IF counter, binary counter C19 to C0	• Data latching the content of IF counter (20-bit binary counter) C19 ← MSB of binary counter C0 ← LSB of binary counter	CTE GT0 GT1

Serial data input (IN1/IN2) t SU, tHD, tEL, tES, tEH ≧ 0.75 μs t LC < 0.75 μs

① CL: Normally HI

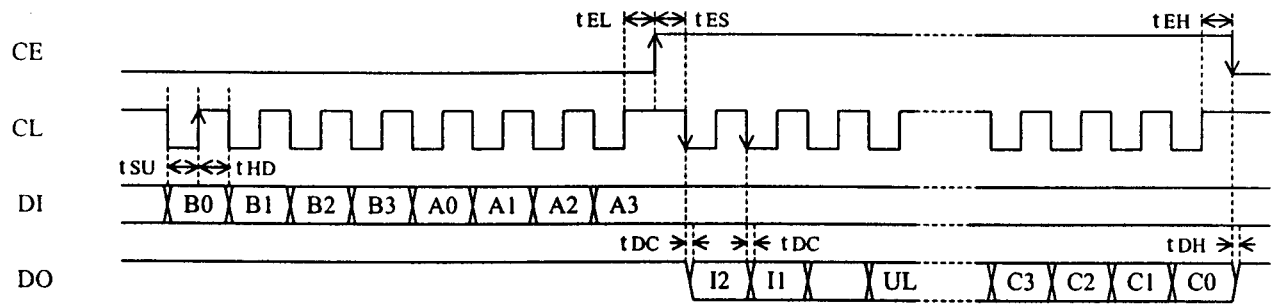


② CL: Normally LOW

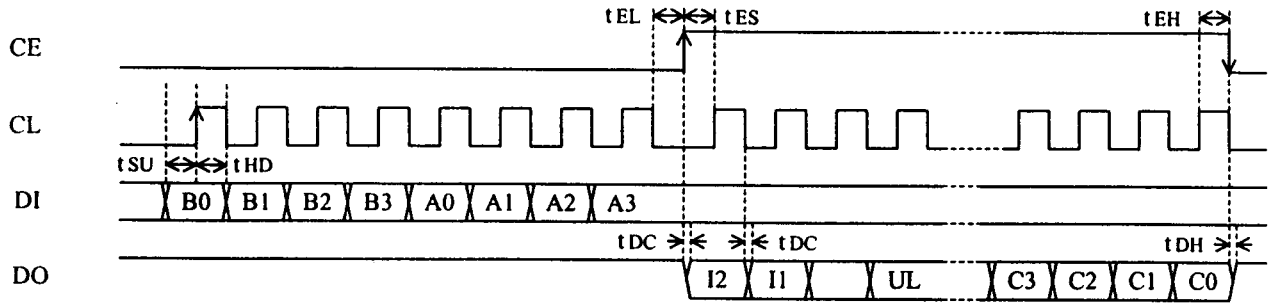


Serial data output (OUT)tSU, tHD, tEL, tES, tEH ≧ 0.75 μs tDC, tDH < 0.35 μs

① CL: Normally Hi

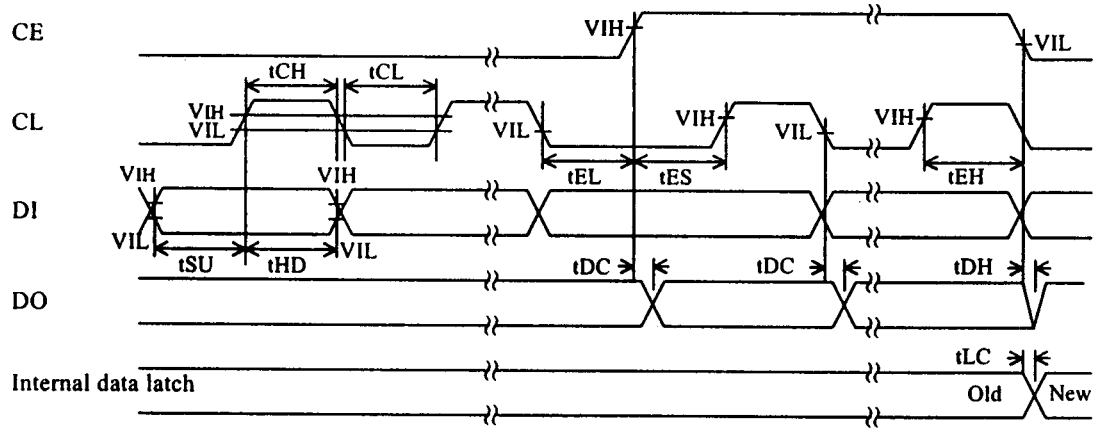


② CL: Normally low

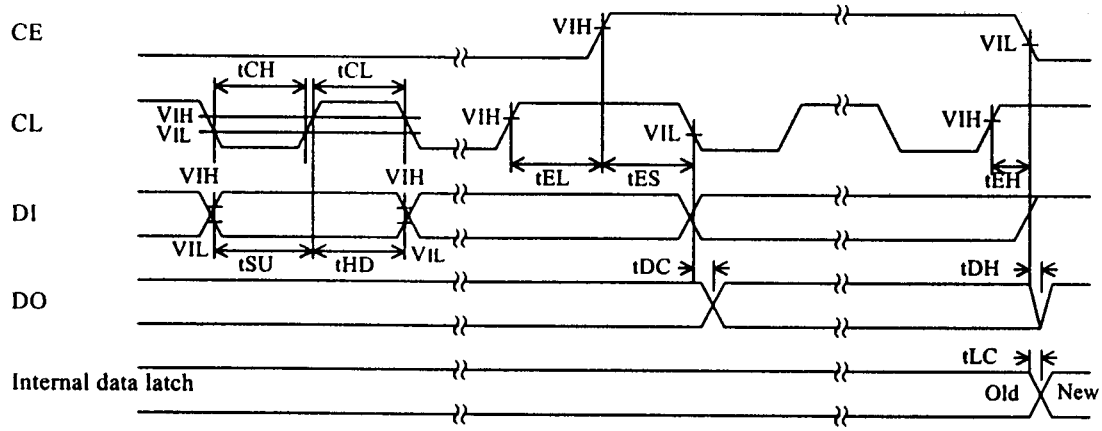


(Note) DO pin is an Nch open drain pin, so that the data varying time (tDC and tDH) differs depending on the pull-up resistance and substrate capacity.

Serial data timing



<< When CL stops at the "L" level >>



<< When CL stops at the "H" level >>

Parameter	Symbol	Pin	Conditions	Min	Typ	Max	Unit
Data setup time	tSU	DI,CL		0.75			μs
Data hold time	tHD	DI,CL		0.75			μs
Clock "L" level time	tCL	CL		0.75			μs
Clock "H" level time	tCH	CL		0.75			μs
CE wait time	tEL	CE,CL		0.75			μs
CE setup time	tES	CE,CL		0.75			μs
CE hold time	tEH	CE,CL		0.75			μs
Data latch change time	tLC					0.75	μs
Data output time	tDC	DO,CL	Differs depending on the pull-up resistance and substrate capacity			0.35	μs
	tDH	DO,CE					

最新カスタムIC搭載により容積30%減（当社従来品比）の小形化を実現。
30 % less volume than our traditional models thanks to state-of-the-art customized IC.

■特長
- 独自開発のICを搭載し、当社従来品容積比約30%減の小形化（60ml）を達成。
- ANTコネクタ部を直出構造とし、内部をフルシールド化することにより、優れたノイズ除去能力を発揮。

■用途
- マイクロコンポーネントステレオ、MDラジカセ、DVD、オーディオレシーバなど多機能化、小形化傾向の進む、各種オーディオ機器、ミニコンポーネントステレオ、各種多機能オーディオ機器。

■Features
- Uniquely developed IC has achieved a small volume of 60 ml, 30 % less than our traditional models.
- Fully shielded structure with ANT connector effectively filters out noise.

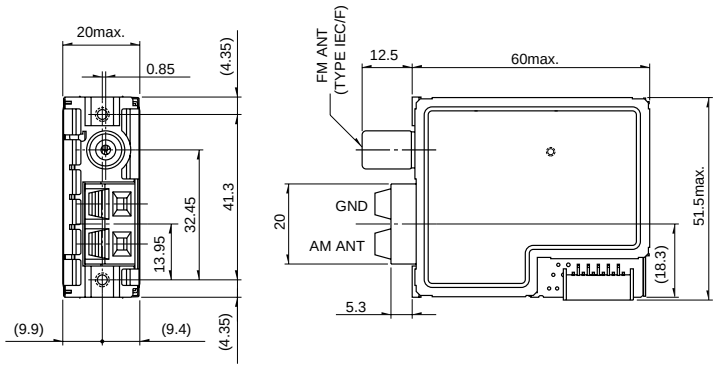
■Applications
- Offers a wide range applications to audio equipment, especially multi-functional, compact audio equipment, such as mini- and micro-component stereo equipment, MD radio cassette recorders, DVDs and audio receivers.

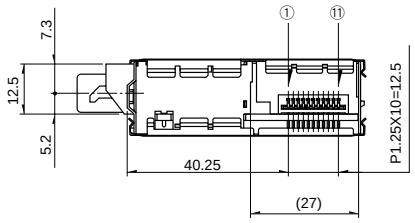
■主な仕様　Typical Specifications

Items			Specifications
Receiving frequency range	AM	(kHz)	530 to 1710
	FM	(MHz)	87.5 to 108
Input impedance (Ω)	AM		—
	FM		75
Receive sensitivity (dBμ)	AM@SN20dB		51
	FM@SN50dB		15
Stereo separation (dB)	FM		45
Output level (dBs)	AM		−7.5
	FM		2.5
Total harmonic distortion (%)	AM		1.2
	FM		0.25
Power consumption		(V/W)	9/500
Volume		(ml)	60

■外形図　Dimensions

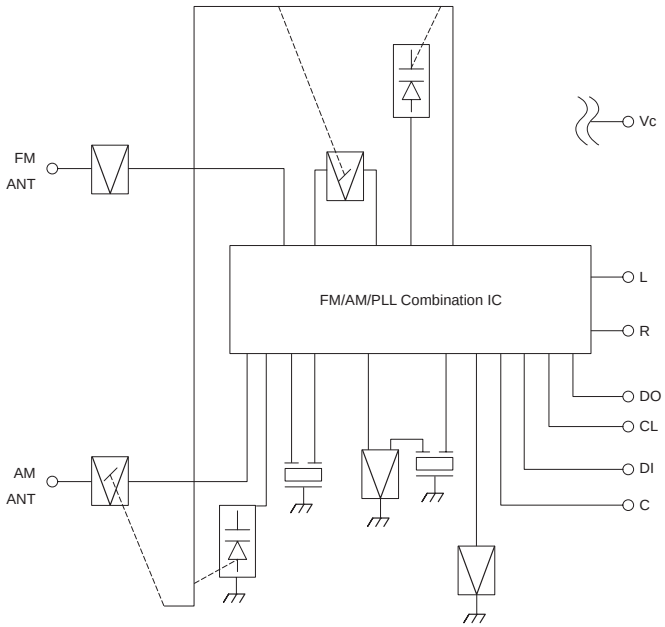
Unit : mm





Terminal No.	Terminal name
①	GND
②	FM DET
③	VSM
④	Rch OUT
⑤	Vcc
⑥	Lch OUT
⑦	GND
⑧	DO
⑨	CL
⑩	DI
⑪	CE

■回路ブロックダイヤグラム　Circuit Block Diagram



SPEAKERS PART

DK1005S Principles and Maintenance

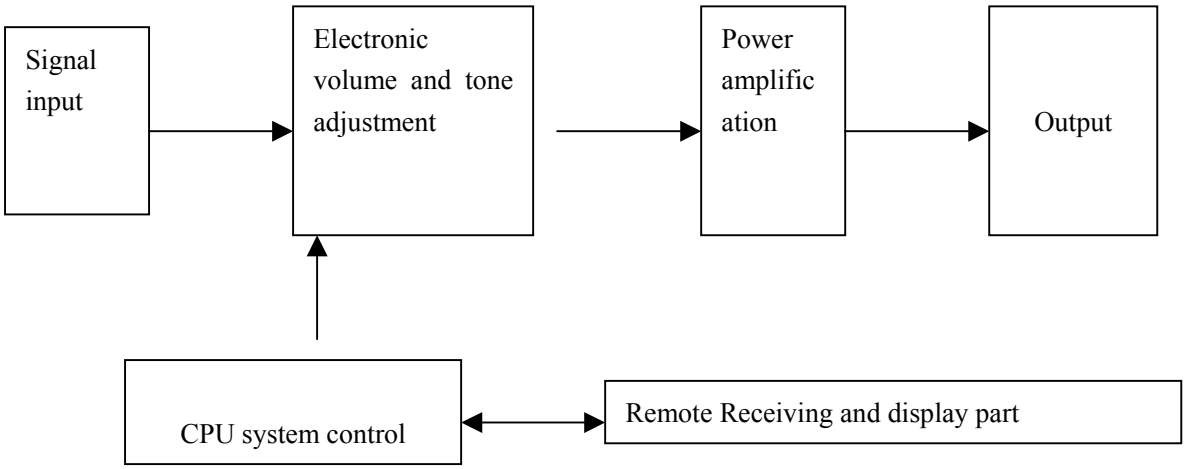
DK1005S is a medium-grade active sound box consisting of one subwoofer sound box, two pre-positioned satellite sound boxes, two surround sound boxes and one centrally positioned sound box. The product features good sound effect in appropriate space, and it has the following features:

1) 2.1/5.1 sound channel output;

2) Built-in five sound channel power amplification, and adaptable to AC-3/DTS and stereo music replay;

3) Six sound channel volume control and independent level control, with tone adjustment function.

二、Principle block diagram



三、 System composition

The device comprises input board, output board, power amplification board and control panel. The input board and output board only consist of

a few terminals. The power amplification board is the most important part, fulfilling control, amplification and power supply for the whole system. In the following is the brief description of the principles for the power amplification board.

1、 Power supply part

In consideration of the big output power of the subwoofer, the device employs a ring transformer for power supply. A group of 18V(AC) voltages is output from the transformer, which will be subject to rectification and filtering and will output +22 V voltage to power IC TDA8947 and IC TFA9843 for power supply.

One line of output 22V voltage goes through the current limiting resistor R101, voltage regulating diode VD104 and capacitor C108 and then output +9V voltage to IC 75347; the other line goes through R100 and voltage regulating diode VD105 and then output 5V voltage power supply for the CPU and the control panel.

2. Signal input, volume adjustment

The device has six channels for signal input. The signals input through each channel will go through the filtering capacitor before being directly delivered to the IC TDA7448 for volume adjustment. In addition, one line of signals will be derived from the L and R main sound channels and overlapped on the SW input. As a result, 2.1 output result will be

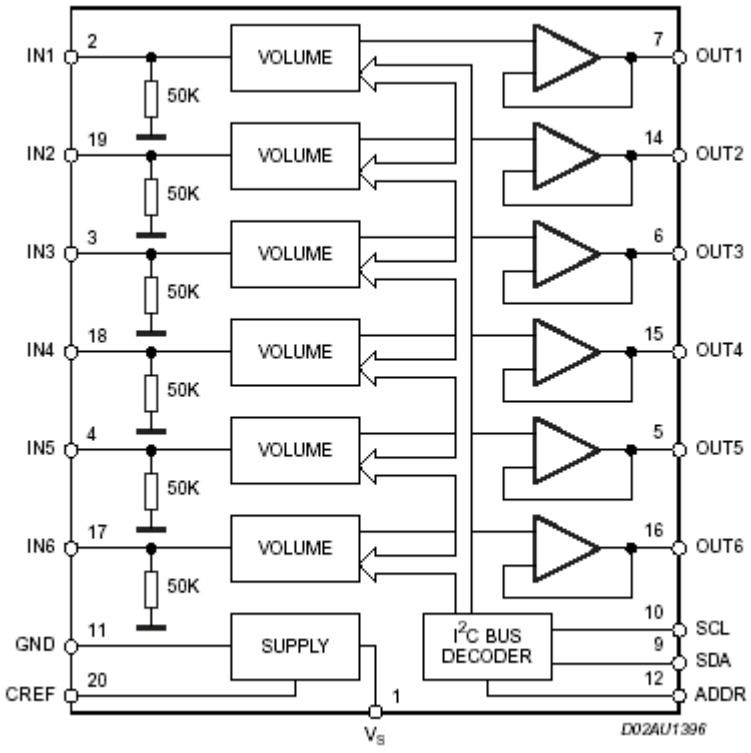
achieved even when there are only L and R sound channel inputs.

IC TDA7448 is an IC with six-channel independent volume adjustment. With its gains adjustable from 0 to 79 single DB, it is applicable to home theater products. With benefits such as small range of power supply, low power consumption and wide temperature scope, it is a quite competent IC, and the functions of its main pins are listed in the following table:

Pin name	Pin Numbering	Function description
IN1	2	Signal input
IN2	19	Signal input
IN3	3	Signal input
IN4	18	Signal input
IN5	4	Signal input
IN6	17	Signal input
OUT1	7	Signal output
OUT2	14	Signal output
OUT3	6	Signal output
OUT4	15	Signal output
OUT5	5	Signal output
OUT6	16	Signal output
GND	11	Grounding pin
CREF	20	Reference voltage

VS	1	Power voltage
SCL	10	Clock control line
SDA	9	Data control line
ADDR	12	Digital voltage

The IC principle diagram is illustrated in the following figure:



2、 Amplifying circuit part

Principle: as far as the signals output from the IC 7448 are concerned, the signals of the main sound channel will be delivered to the N101 IC TFA9843 for power amplification; the central surround signals will be filtered and delivered to the N106 IC TDA8947 for amplification; the subwoofer signals will first pass experience amplitude limit (the amplitude limit circuit comprises VD110 and VD113 diodes) and pretreatment before being delivered to the N102 IC TFA9843. Amplitude

limit is aimed at preventing excessive size of signals, which may, after amplification, damage the loudspeaker due to excessive power. Because the power supply of the amplification IC is fulfilled by a single power source, all amplified and output signals will have DC, therefore, the signals will still experience filtering before being output to the loudspeaker.

IC TFA9843J is used for dual sound channel power amplification. With standby and mute modes, free from switch impact, and with functions such as short circuit protection and overheat protection, it can effectively be prevented from being damaged in case of IC abnormality. In ordinary output mode, the IC can supply for each channel a maximum of 20W power output. When BTL output is employed, the power can be as high as 40W. In addition, the IC features powerful anti-ripple performance, with little power consumption in the standby state.

The functions of the various pins of the IC TFA9843J are listed in the following table:

Symbol	Pin	Function
IN2+	1	2nd channel input
OUT2-	2	2nd channel output
CIV	3	Common mode input voltage suppression

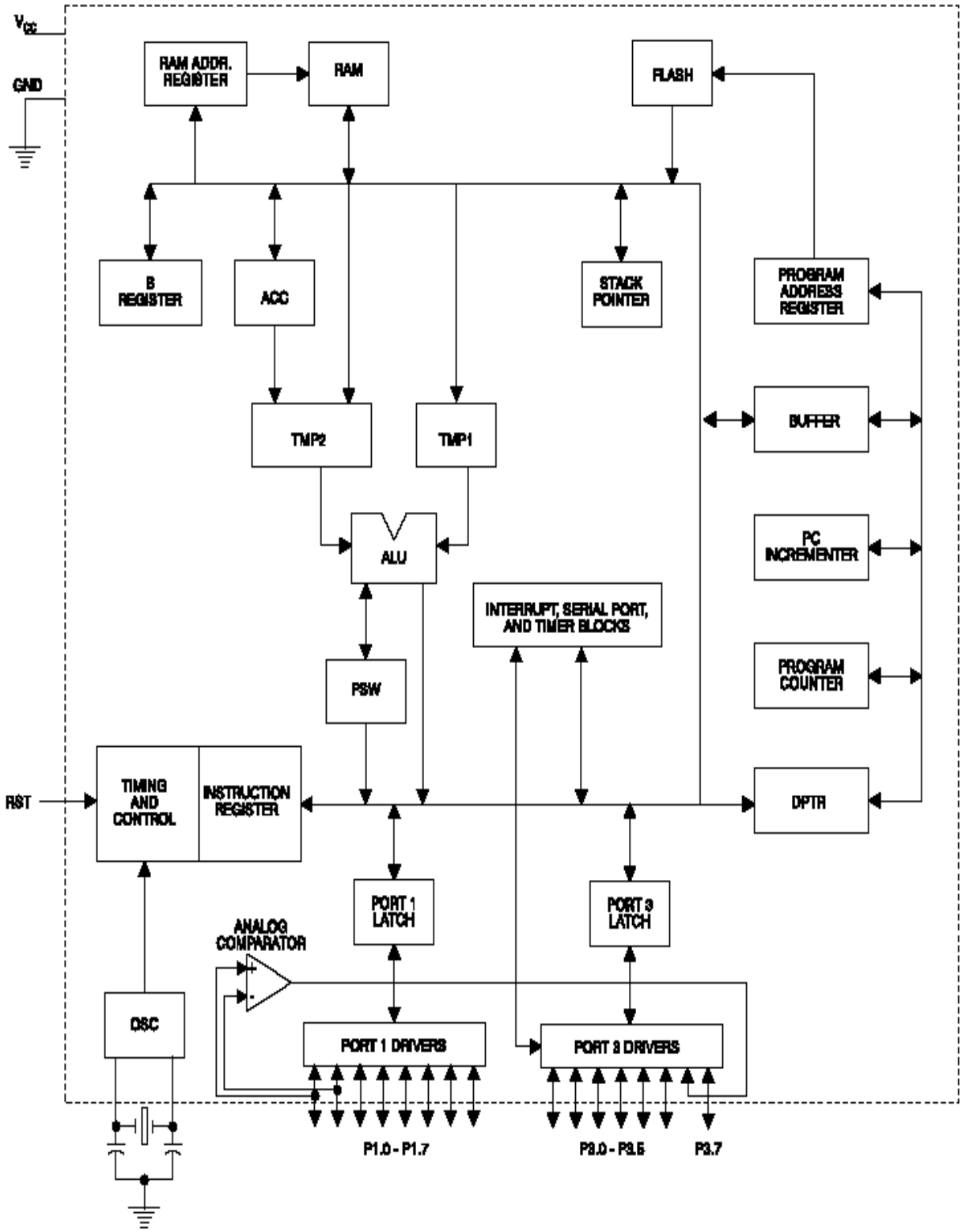
1N1+	4	1st channel input
GND	5	Ground
SVR	6	Reference voltage
MODE	7	Mode selection
OUT1+	8	1st channel output
VCC	9	Power supply

IC TDA8947J is used for four channel power amplification. Its features are similar to those of the IC TFA9843J, however, its output power is bigger, and a single sound channel can be as high as 25 W.

3、 Control circuit

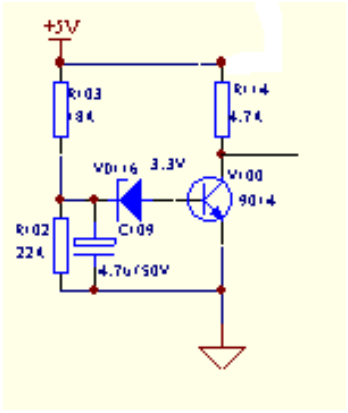
The device employs IC AT89C2051 to serve as its core part to control the operation of the whole device. With low voltage and high performance, it employs 8-bit 2K bytes flash and ROM single-chip. Boasting 15 I/O ports and six interrupt sources; it has features such as low power consumption and standby mode.

The principle block diagram of the IC is illustrated in the following figure:


V_{CC}
GND
RAM ADDR. REGISTER
RAM
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
ANALOG COMPARATOR
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.5
P3.7

Reset circuit:

The device employs high level for resetting. By making use of the feature of the capacitor C109 that there is no jump for of voltage, the device ensures that there is no jump of capacitor voltage at the instant of power on. The base electrode of the triode V100 has low level, so that the triode is not on, and the 5V voltage is added to the first pin of the CMP through resistor R114. With capacitor charging, the positive voltage of the capacitor gradually climbs; when the voltage attains a certain limit, the voltage regulating diode is reversely on, so that the base electrode of the triode has high level, the triode is on, the reset pin voltage turns into low level, thus fulfilling resetting. The circuit diagram is illustrated in the following figure:



Reset circuit

Mainly remote control is employed for adjustment of the status of the device. The signals received by the remote controller are delivered to the sixth pin of the CPU. After the signals are processed inside the CPU, pins 8 and 9 deliver control signals to adjust the volume of the device. Then there will be corresponding display on the control panel through P1 port,

so that users are able to understand the status of the device. In addition, pins 2 and 3 of the CPU are used to control the mute state of the main sound channel and the central surround.

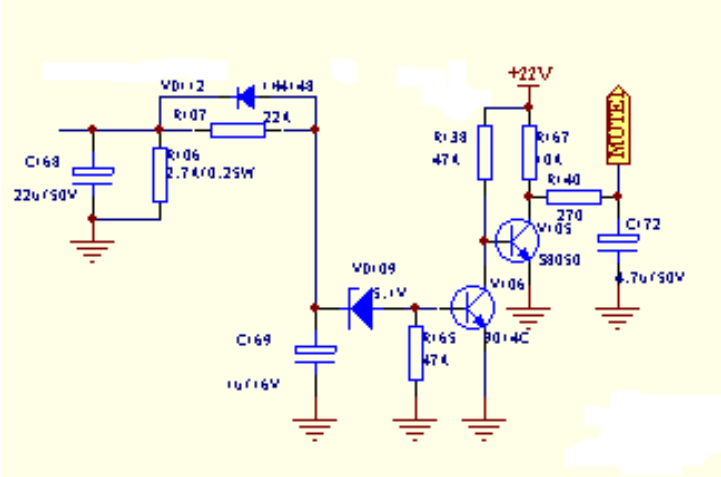
5. Control panel

The control panel of the device consists of a remote control receiver and a nixie tube. Because the device is operated through remote control, the remote control receiver is the sole path for man-machine communication. The nixie tube is used to display the ongoing operation and the state of the whole system.

6. Power on/off mute and mute circuit

Power on/off mute: as shown in the figure, at the instant of power on, the voltages on both sides of capacitor C169 won't experience jump-off, as a result, the low level will remain unchanged, the triode V106 is off, V105 is on, MUTE1 output turns into low level, LRM and SCM signal levels turn lower, and then there is mute. When the capacitor is charged to turn on VD109 5.1V voltage regulator tube and V104 9014 triode, the level of the V105 base electrode will become lower, so that triode V105 turns off, MUTE1 outputs high level, and the mute then comes to an end. The same case applies to power off. Capacitor C169 experiences fast discharge through diode VD112, so that the positive voltage experiences fast decrease, triode V106 turns off, V105 turns on, MUTE outputs low

level and turns on. It is through this circuit that we achieve no impact sound when power is on/off.



Mute circuit: the mute function is realized through the mute signals transmitted by the CPU. Press the MUTE key on the remote controller, the remote control receiver will receive signals and transmitted them to the CPU for processing. Then, pins 2 and 3 of the CPU will transmit high level, so that triodes V107 and V108 turn on, LRM and SCM levels become lower, and the mute is on. It makes use of the mode selection feature of the IC TDA9843 and IC TDA8947. For more details, please refer to the information for the IC TDA9843.

四、 Troubleshooting

The electronic circuit inside the device is relatively simple, without too many complicated control and detection circuits. As a result, signal injection method is employed for the maintenance of the device, namely, signals are added to the input end, and flow along the signal procedure. If

signals are interrupted at a certain place, then we can determine that the fault may happen here.

The maintenance of the device is in compliance with the following procedures:

1、 Check whether the power supply part is normal, namely, check whether the power supply of 22V, 9V and 5V is normal;

2、 In case of abnormal sound but normal power supply, check whether the mute level is normal, and then consider whether it is attributed to the wrongness of other parts;

3、 For a device with abnormal display, first determine whether there is anything wrong with the nixie tube, and then check whether there is anything wrong with the CPU.

**********ATTACHMENT**********

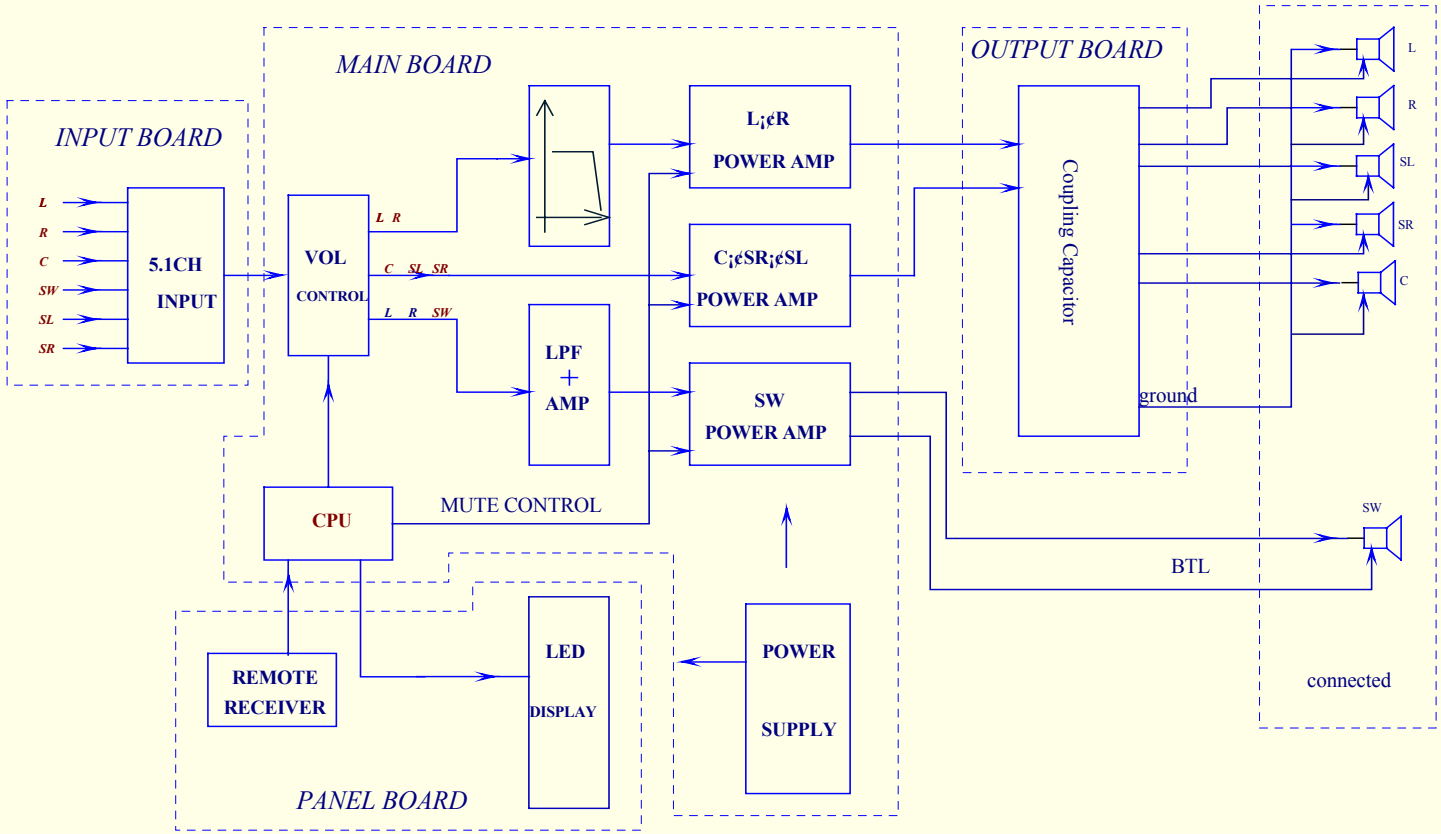
1: Block diagram

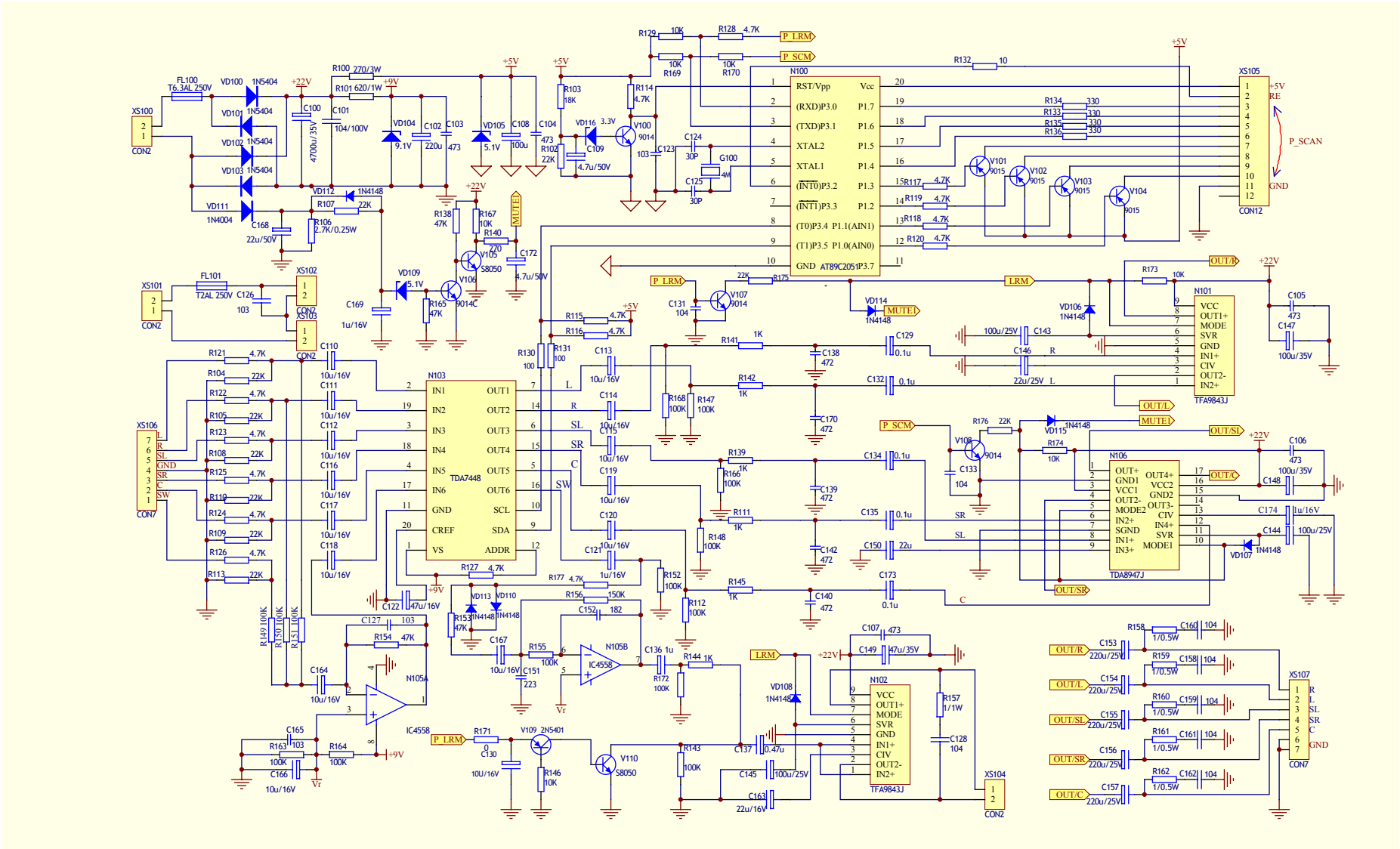
2: Electronic diagram

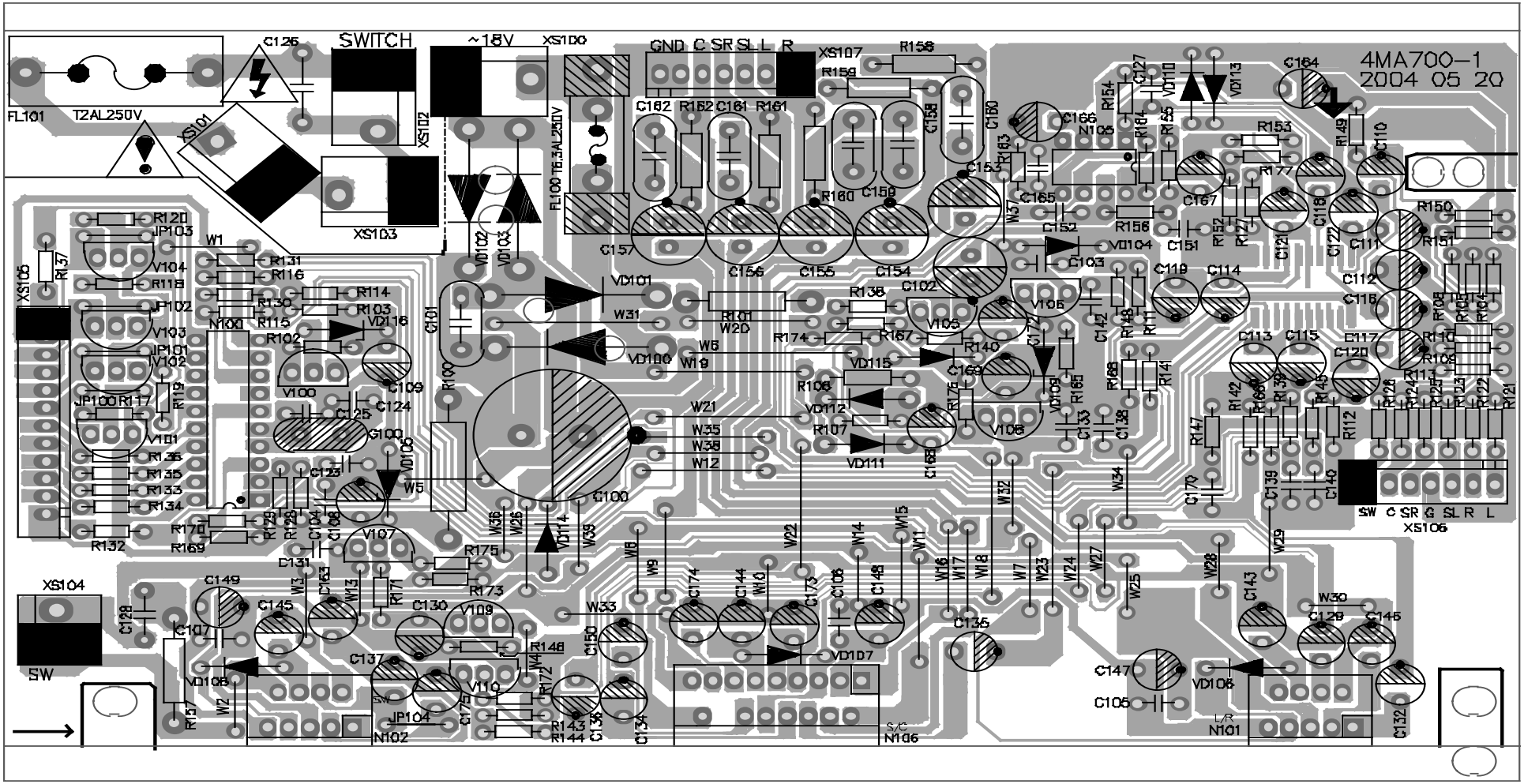
3: PCB silk screen

4: IC specifications

CONNECTED BLOCK



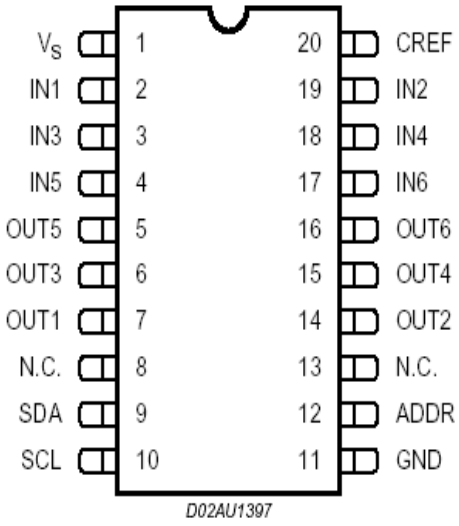

N100
RST/Vpp
(RXD)P3.0
(TXD)P3.1
XTAL2
XTAL1
(INT0)P3.2
(INT1)P3.3
(T0)P3.4 P1.1(AIN1)
(T1)P3.5 P1.0(AIN0)
GND AT89C2051P3.7
Vcc
P1.7
P1.6
P1.5
P1.4
P1.3
P1.2
P_LRM
P_SCM
P_SCAN
XS105
CON12
N103
TDA7448
IN1
IN2
IN3
IN4
IN5
IN6
GND
CREF
VS
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
SCL
SDA
ADDR
N101
TFA9843J
N102
TFA9843J
N106
TDA8947J
XS106
CON7
XS107
CON7
XS100
XS101
XS102
XS103
XS104
CON2
IC4558
N105A
N105B
MUTE1
OUT/R
OUT/L
OUT/SL
OUT/SR
OUT/C
+5V
+9V
+22V
Vr
GND


4MA700-1
2004 05 20
SWITCH
~18V
GND C SR SL L R
FL101
T2AL250V
XS101
XS102
XS103
XS100
XS107
XS104
SW
XS105
XS106
SW C SR G SL R L
S/C
N106
L/R
N101
N102
JP100
JP101
JP102
JP103
JP104

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature	-10 to 85	°C
T_{stg}	Storage Temperature Range	-55 to 150	°C

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pin}$	thermal Resistance junction-pins	150	°C/W

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	4.75	9	10	V
V_{CL}	Max Input Signal Handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f =1KHz		0.01	0.1	%
S/N	Signal to Noise Ratio Vout = 1Vrms		100		dB
S_C	Channel Separation f = 1KHz		90		dB
	Volume Control (1dB step)	-79		0	dB
	Mute Attenuation		90		dB

ELECTRICAL CHARACTERISTCS (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, unless otherwise specified0

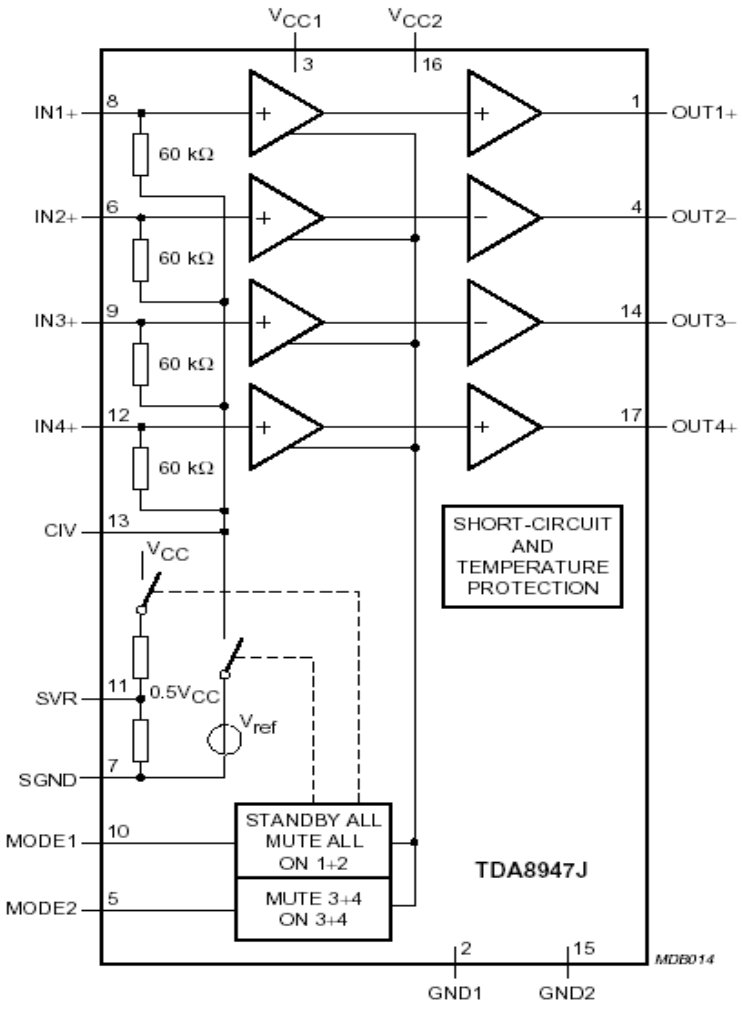
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		4.75	9	10	V
I_S	Supply Current			7		mA
SVR	Ripple Rejection			80		dB
INPUT STAGE						
R_{IN}	Input Resistance		35	50	65	KΩ
V_{CL}	Clipping Level	THD = 0.3%	2	2.5		Vrms
S_{IN}	Input Separation	The selected input is grounded through a 2.2µ capacitor		90		dB
VOLUME CONTROL						
C_{RANGE}	Control Range			79		dB
A_{VMAX}	Max. Attenuation			79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	A_V = 0 to -24dB	-1	0	1	dB
		A_V = -24 to -79dB	-2.0	0	2.0	dB
E_T	Tracking Error	A_V = 0 to -24dB	-1	0	1	dB
		A_V = -24 to -79dB	-2	0	2	dB
V_{DC}	DC Step	adyacent attenuation steps	-3	0	3	mV
A_{mute}	Mute Attenuation			90		db
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	THD = 0.3%	2	2.5		Vrms
R_L	Output Load Resistance		2			KΩ
V_{DC}	DC Voltage Level			4.5		V
GENERAL						
E_{NO}	Output Noise	BW = 20Hz to 20KHz All gains = 0dB, Flat		10	15	µV
S/N	Signal to Noise Ratio	All gains = 0dB; V_O = 1Vrms		100		dB
S_C	Channel Separation left/Right		80	90		dB
THD	Distortion	A_V = 0; V_I = 1Vrms		0.01	0.1	%
BUS INPUT						
V_{II}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Achnowledge	I_O = 1.6mA		0.4	0.8	V

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		9	18	26	V
		no (clipping) signal	[1]	-	-	28	V
I_q	quiescent supply current	V_{CC} = 18 V; R_L = ∞		-	100	145	mA
I_{stb}	standby supply current			-	-	10	µA
$P_{o(SE)}$	SE output power	THD = 10 %; R_L = 4 Ω					
		V_{CC} = 18 V		7	8.5	-	W
		V_{CC} = 22 V		-	14	-	W
$P_{o(BTL)}$	BTL output power	THD = 10 %; R_L = 8 Ω					
		V_{CC} = 18 V		16	18	-	W
		V_{CC} = 22 V		-	29	-	W
THD	total harmonic distortion	SE; P_o = 1 W		-	0.1	0.5	%
		BTL; P_o = 1 W		-	0.05	0.5	%
$G_{v(max)}$	maximum voltage gain	SE		25	26	27	dB
		BTL		31	32	33	dB
SVRR	supply voltage ripple rejection	SE; f = 1 kHz		-	60	-	dB
		BTL; f = 1 kHz		-	65	-	dB

[1] The amplifier can deliver output power with non clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.



4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	operating	9	18	26	V
		no signal	-	-	28	V
I_q	quiescent supply current	V_{CC} = 18 V; R_L = ∞	-	60	100	mA
I_{stb}	standby supply current		-	-	10	µA
P_o	SE output power	THD = 10 %; R_L = 4 Ω; V_{CC} = 18 V	7	8.5	-	W
		THD = 10 %; R_L = 4 Ω; V_{CC} = 22 V	-	14	-	W
	BTL output power	THD = 10 %; R_L = 8 Ω; V_{CC} = 18 V	16	18	-	W
		THD = 10 %; R_L = 8 Ω; V_{CC} = 22 V	-	29	-	W
THD	total harmonic distortion	SE; P_o = 1 W	-	0.1	0.5	%
		BTL; P_o = 1 W	-	0.05	0.5	%
G_v	voltage gain	SE	25	26	27	dB
		BTL	31	32	33	dB
SVRR	supply voltage ripple rejection	SE; f = 1 kHz	-	60	-	dB
		BTL; f = 1 kHz	-	65	-	dB

Block diagram